Material-Centric Modeling of PWB Fabrication: An Economic and Environmental Comparison of Conventional and Photovia Board Fabrication Processes

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***Abstract*—This paper presents an activity-based cost model for printed wiring board (PWB) fabrication in which the process steps are defined by material processing activities. The model is designed to be used during system planning and tradeoff analysis prior to physical design. In many activity-based manufacturing cost models, activities are based on equipment and facilities ("equipment-centric"). In the present model, the process steps are based on material processing activities ("material-centric"). Equipment-centric models are appropriate for integrated circuit (IC) manufacture where the processing cost is driven by facilities and equipment; however, in PWB manufacturing, where a significant portion of the cost is materials, it is more appropriate to focus the process modeling around material activities.**

The models presented in this paper compute the volume of materials used and wasted by the activities associated with the fabrication of PWB's, and in turn, use the computed volumes as inputs for predicting fabrication and waste disposition costs. Activities included in the model are open- and closed-loop plating, coating, etching, stripping, desmearing, plasma etching, lamination, drilling, filling, singulation, and scrapping. Additionally, waste disposition activities that operate on the waste inventory are supported. The models presented here have been integrated into a software tradeoff environment that concurrently performs cost and performance analysis for electronic systems.

A tradeoff study is presented that compares the cost and waste associated with fabricating mechanically drilled and plated through-hole PWB's with conventional and alternative resists and two fully-additive photolithographic microvia PWB fabrication processes.

***Index Terms*— Cost modeling, design-for-environment (DFE), design-to-cost, material-centric analysis, microvia PWB's, printed wiring board (PWB), tradeoff analysis.**

I. Introduction

An important part of understanding an electronic system's cost is the accurate prediction of the cost of the substrate on which the electronic application is interconnected. The development of cost-of-ownership (COO) models for modeling integrated circuit (IC) fabrication [1] and electronic system assembly have been instrumental in bringing about an understanding and appreciation of activity-based costing methods that are directly tied to specific process steps. Accurate cost prediction of the printed wiring board (PWB) fabrication process has both similarities and differences with respect to cost modeling for IC fabrication and electronic system assembly. All three manufacturing activities are process flow/activity-based oriented, have labor, material, tooling, and equipment/facilities contributions, and may be performed for single parts or in multi-up array formats. However, the significant cost drivers are not the same for PWB fabrication as for IC fabrication and electronic system assembly. COO approaches for IC fabrication tend to focus on computing the lifetime cost to own and operate specific equipment and the equipment's impact on the process, as these are the cost drivers in the IC industry. While the cost of materials is included in these models, it is not the focus of the analysis and the ability to perform detailed material manipulation is typically not emphasized. In contrast, the cost of PWB fabrication is driven almost exclusively by materials (in some cases more than 50% of the cost of a PWB is material cost). Labor cost is the second largest cost driver and equipment is a distant third. Even significant changes in equipment and facilities costs (including maintenance, down-time, etc.) typically do not have a large impact on the final board cost.

Both IC fabrication and PWB fabrication differ from other industries, including electronic assembly, in the importance of accounting for waste. The amount of waste generated during the fabrication of IC's and PWB's significantly exceeds the amount of material in the final fabricated chip or board, with a large portion of the waste considered hazardous. In conventionally fabricated PWB's, up to five times more waste than product (by weight, not including water) is generated during the board production process [2]. Managing and disposing of this waste can represent up to 10% of the cost of a board. Therefore, it has become important that PWB manufacturers consider the costs associated with the waste stream created when boards are fabricated. While there are material inventory models that have more rigorous material accounting systems than the approach presented here (lifecycle analysis methods are discussed in Section II) they generally do not tie in waste handling costs or allow for detailed computation of waste as

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a function of process or design and are less than optimum for analysis of PWB fabrication cost and inventory.

A. The Material-Centric Concept

In a material-centric PWB fabrication model, each activity or process step is defined in terms of what it does to the materials associated with the substrate being fabricated. Five fundamental activities are used in this model:

1) *Additive*—activities that add material to the product.
   Instances:
   a) plating;
   b) coating;
   c) lamination;
   d) filling.
2) *Subtractive*—activities that subtract material from the product.
   Instances:
   a) etching;
   b) stripping;
   c) drilling;
   d) trimming (singulation).
3) *Waste Disposition*—activities that operate on the materials in the waste stream.
4) *Scrapping Defective Parts*—activities that add partial or complete parts to the waste stream.
5) *Activities with no material manipulation*.

In addition, activities 1)–4) may have associated "consumable" materials. We are defining consumables as materials that are attached to the process (as opposed to the product). Consumables are used and "worn out" by the activities and therefore have a limited lifetime. This lifetime may be a single use (e.g., water) or many uses (such as developer, artwork, drill bits). Lifetime may be defined as a fixed amount of time (one week, six months) or by volume of product processed. Consumable materials are always completely wasted and at no point in the process do they reside in the product.[1]

While process steps that model the above material activities contain information about the equipment and facilities required, the process steps are not defined by the equipment and facilities. By defining process steps in terms of their material treatment, modeling of material usage and waste costs becomes straightforward.

B. Cost and Waste Modeling for Tradeoff Analysis

All the methods presented in this paper are designed for use during system-level planning and technology tradeoff activities that take place prior to physical design (layout and routing) of the board. Alternative methodologies that predict cost, material usage and waste after physical design of the board fit the traditional "correct-by-verification" paradigm, in which cost and environmental ramifications of an electronic product are not quantitatively assessed until the design is nearly completed. Because certain system attributes can not be added (or are very expensive to add) after the design is completed, modern design aspires to be "correct-by-design."

A correct-by-design approach depends on the automation of system planning and synthesis. The key to the planning/synthesis activity is design optimization, i.e., automating the process of performing interdisciplinary design tradeoffs. In an ideal design flow, design-to-cost (DTC) and design-for-environment (DFE) activities are part of the broader interdisciplinary tradeoff methodology. While independent DTC and DFE activities are useful, their value to system designers can not be fully realized unless the impact of DTC and DFE decisions on other system economic and performance measures (i.e., electrical and thermal performance, reliability, size, etc.) can be accurately assessed.

This paper presents a methodology for incorporating materials (resident in the product and wasted) within a detailed activity-based cost model that is part of a larger interdisciplinary tradeoff analysis methodology [4].

II. Modeling Materials Used and Wasted

The cost modeling described in this paper was implemented in an activity-based cost analysis, enhanced with energy/mass balance. The cost model resides in an existing interdisciplinary tradeoff analysis tool for multichip systems [4]. Energy estimation and inventorying were discussed in [5] and therefore will not be addressed again here. This section focuses on PWB manufacture; however, the principles described are generally applicable to other substrate technologies. Similar analytical modeling of the volume of material wasted in major PWB fabrication activities appears in [6]. Other broader, lifecycle analysis (LCA) methodologies, predict material usage and waste at a more general level with minimal design specific information, [7]. None of the alternative methodologies mentioned above are intended for cost modeling or have any significant economic modeling capabilities. Two known efforts are attempting to marry LCA concepts with cost analysis. EcoBoard [8], is a tool that estimates environmental impact considering product manufacture and downstream processes. A methodology that marries conventional LCA energy/mass balance with COO cost analysis for IC wafer fabrication has been reported in [9].

A. Inventory Dynamics

During the execution of a process flow, inventories of material in the product, material in the waste stream, and energy consumed are created and manipulated. Each material inventory catalogs the material's volume at standard temperature and pressure (STP) and the material's name. As each process step is executed, its material and energy requirements are computed and added to, or subtracted from the appropriate inventories. Some activities transfer materials between inventories, e.g., if the step produces waste materials by removing material from the product, the quantity of waste is subtracted from the material used inventory and added to the material waste inventory. All the inventories are normalized to

[1] We are using a broader definition of consumables than SEMI. SEMI defines consumables as, "all parts of the equipment that are worn out by the process operation of equipment and require replacement after less than one year of operation" [3]. The SEMI definition would not include water.

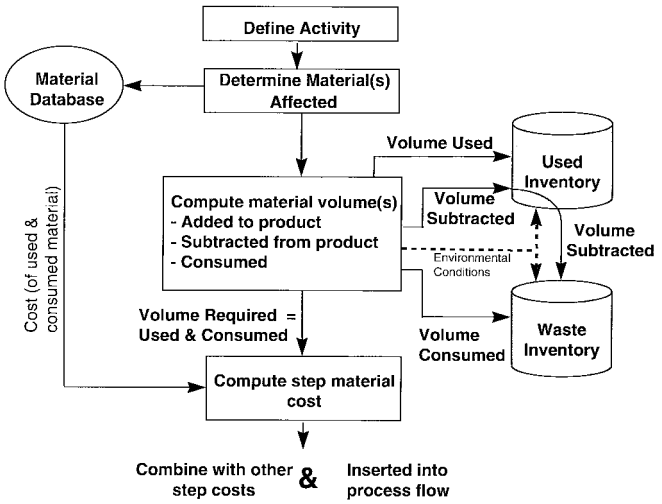

Fig. 1. Modeling process for treating material addition and subtraction. The environmental conditions are necessary to convert the material volumes to STP. The material database provides material cost and waste disposition information.

one instance of the part being processed, i.e., the inventories keep the used and wasted materials that correspond to a single panel or board. If the total waste is desired, the contents of the waste inventory must be multiplied by the number of panels or boards that remain in the process.

The interaction of the inventories with the process flow for the basic additive and subtractive material-centric activities is shown in Fig. 1. The models that support the computation of material volumes in Fig. 1 are discussed in the next subsection.

B. Material Use and Waste Models

When a process step is executed, the quantity of material used and/or wasted by the step is automatically computed. The computed volumes are converted to volume at STP for storage in the used and waste inventories. The following general parameters are used in the proceeding discussion:

$\text{volume}_{\text{used}}$ = volume of material (per panel or board) that leaves the process step with the part being processed

$\text{volume}_{\text{wasted}}$ = volume of material (per panel or board) that is sent into the waste stream

$\text{inventory}_{\text{wasted}}$ = inventory of the materials (and their associated volumes) in a single panel or board

$\text{inventory}_{\text{wasted}}$ = inventory of the waste materials (and their associated volumes) allocated per panel or board.

The inventories correspond to panels prior to singulation into boards, and are automatically mapped to correspond to boards after the singulation activity. Algorithms for computing the number of boards on a panel (number-up) are discussed in [10].

1) Plating, Coating, and Wet Cleaning: Plating, coating, and wet cleaning activities may be treated as open- or closed-loop systems. In the open-loop system, materials used to perform the activity are used only once before being disposed of (e.g., nonrecirculated spray or curtain coat). A closed-loop system assumes that the material used to perform the activity is reusable (e.g., bath, recirculated spray, or curtain coat).

It is assumed that there is no material used in cleaning steps (i.e., no material leaves the process step with the product). For both open- and closed-loop systems, the material used in *plate* and *coat* steps is given by

$$\text{volume}_{\text{used}} = (\text{area})(\text{thickness}) \tag{1}$$

where

$$\text{area} = \text{panel or board area}$$
$$\text{thickness} = \text{layer thickness}.$$

Equation (1) is the simplest estimation; however, more detailed estimations associated with a specific process can also be used. For example, the volume used in a curtain coat activity would depend on the speed at which the part moves through the curtain.

Material wasted applies to *plating, coating,* and *cleaning*. The waste associated with open-loop system activities is

$$\text{volume}_{\text{wasted}} = (\text{flow rate})(\text{time}_{\text{part}}) - \text{volume}_{\text{used}} \tag{2}$$

where

$$\text{flow rate} = \text{rate of material flow in the open-loop system}$$
$$\text{time}_{\text{part}} = \text{the amount of flow time allocated to each part.}$$

The waste material from steps that are characterized as closed-loop systems is given by the volume of the closed-loop system that is wasted per part

$$\text{volume}_{\text{wasted}} = \frac{(\text{area})(\text{bath volume})}{(\text{maximum surface area per bath})} - \text{volume}_{\text{used}} \tag{3}$$

where the denominator of (3) is the lifetime of the bath measured in the maximum surface area the bath can process before it is discarded. If the life of the bath is characterized as number of parts processed or time, either measure can be normalized to the effective surface area processed.

Unfortunately, baths are usually more complex than the characterization in (3). Real baths are often refreshed periodically with additional bath material or specific components of the bath. In order to account for additional bath material used to refresh the bath, the bath volume in (3) is given by

$$\text{bath volume} = \text{bath volume}_{\text{actual}} + \text{bath volume}_{\text{added}} \text{ per life} \tag{4}$$

where the $\text{bath volume}_{\text{added}}$ per life is computed from the bath loss rate (e.g., one might convert 10% volume loss per day to 0.5 gal volume loss per 600 sq. ft. using the actual bath volume and the throughput). Refreshing a single component of a bath requires that the loss rate of the component be known and converted to a component volume/life that can be substituted for bath volume into (3).

2) Etch and Strip: Etching and stripping activities may also be characterized as open- or closed-loop systems when performed as wet processes (typical). However, computing the waste from *etching* or *stripping* activities is complicated by the fact that the etch (or strip) combines with the material that it removes to form new materials that appear in the waste stream. In the simple case, where there are no new compounds formed, the waste generated by *etching* or *stripping* steps is given by

$$\text{volume}_{\text{wasted}} = (\text{area})(\text{plating thickness})(\text{fraction etched}) \quad (5)$$

where the material in the last *plated, coated* or *laminated* layer is etched and the fraction etched is an input provided either by the user or as an automatic input from wiring analysis (see the discussion associated with (16) for more information). The etchant is added to the material waste inventory [computed using (2) or (3)] while the material it removes is subtracted from the material used inventory then added to the material waste inventory. If new compounds are formed by the *etching* or *stripping* process then the etchant indicated by $\text{volume}_{\text{wasted}}$ in (5) is post processed by comparison to a chemical compound database to ascertain the type and quantity of compounds formed.

3) Plasma Etching: Cleaning, etching, stripping, and *desmear* activities can be performed using plasmas (for dry processing). Plasma etching is treated as an open-loop system. The volume of plasma gases used is given by

$$\text{volume}_{\text{wasted}} = (\text{flow rate})(\text{etch time}) \quad (6)$$

where

$$\begin{aligned}\text{flow rate} &= \text{rate of gas usage}\\ \text{etch time} &= \frac{(\text{thickness})}{(\text{etch rate})}\\ \text{thickness} &= \text{thickness of the layer being etched}\\ \text{etch rate} &= \text{the rate at which the plasma removes the material being etched.}\end{aligned}$$

The volume of the panel or board that is etched is computed using the relation in (5).

4) Lamination: The material added through *lamination* (steps that add sheets of material) is computed using (1), with area replaced by the area of the sheet ($\text{area}_{\text{sheet}}$). The waste material associated with lamination is given by

$$\text{volume}_{\text{wasted}} = (\text{area}_{\text{sheet}} - \text{area}_{\text{overlap}})(\text{thickness}) \quad (7)$$

where $\text{area}_{\text{overlap}}$ is the area of the overlap between the panel and the sheet, and thickness is the thickness of the laminate. Equation (7) is only used if the sheet area is greater than the overlap between the sheet and the panel, if the sheet is smaller than the panel, then there is no laminate waste at this point in the process (laminate will be added to the waste stream later, when boards are singulated from the panel).

Equation (7) represents the laminate waste prior to the actual lamination activity. The heat and pressure of the lamination process usually produces an additional flash around the periphery of the part. At some point, the extra flash along with the volume from (7) is trimmed and contributed to the waste stream. The amount of laminate wasted as flash is given by

$$\text{fraction}_{\text{laminate removed}} = (\text{fraction}_{\text{flash}})(\text{volume}_{\text{laminate}}) \quad (8)$$

where $\text{fraction}_{\text{flash}}$ is the fraction of the laminated material that appears as flash and $\text{volume}_{\text{laminate}}$ is the original volume of laminate prior to lamination less the waste volume given by (7). The $\text{fraction}_{\text{flash}}$ may be estimated from the ratio of the layer thickness after lamination to the original laminate thickness. The $\text{fraction}_{\text{laminateremoved}}$ computed above is used to transfer the specific laminate material in the used inventory to the waste inventory as in Fig. 1.

5) Drilling: The waste generated by *drilling* steps is based on the computation of the fraction of the total panel or board area removed

$$\text{fraction}_{\text{removed}} = \frac{\text{area}_{\text{removed}}}{\text{area}} \quad (9)$$

where area is the area of the panel or board being drilled and the $\text{area}_{\text{removed}}$ is computed from

$$\text{area}_{\text{removed}} = (\text{array size})(\text{holes per board})\left[\frac{\pi\ \text{diameter}^2}{4}\right] \quad (10)$$

where

$$\begin{aligned}\text{array size} &= \text{number of board per panel, i.e., number-up}\\ \text{diameter} &= \text{the diameter of holes drilled.}\end{aligned}$$

The length of the holes drilled in the piece is given by

$$\text{hole length} = \frac{\text{fraction}_{\text{removed}}}{\text{area}_{\text{removed}}}\,(\text{volume of inventory}_{\text{used}}) \quad (11)$$

where the $(\text{volume of inventory}_{\text{used}})$ is the total volume of the used inventory. This length is not needed to characterize the drilling process, but may be needed to characterize *desmear*, *hole plating,* and *hole filling* operations later.

The fraction removed, computed in (9), is used to uniformly reduce the material used inventory and to add all of the material removed to the material waste inventory.

An additional source of waste material associated with the drilling process is used drill bits (drill bits are considered a consumable). The waste from drill bits is computed using

$$\text{volume}_{\text{removed}} = (\text{bit length})\left[\frac{\pi\,\text{diameter}^2}{4}\right] \cdot \left[\frac{(\text{holes per board})(\text{array size})}{(\text{bit lifetime})}\right] \quad (12)$$

where bit lifetime = (strokes between retips) (maximum number of retips + 1). The product of the maximum number of retips and the cost per retip is added to the original drill bit cost.

Desmear steps are treated as specialized cleaning activities that operate on all surfaces, specifically the inside of holes by

removing material that smears during the drilling process. The volume of the material removed by desmearing is given by

$$\begin{aligned}\text{volume}_{\text{removed}} &= (\text{smear thickness})(\text{surface area}_{\text{holes}}) \\ &\quad + (\text{plating thickness})(\text{fraction etched}) \\ &\quad \cdot \left[\text{area} - \frac{\pi\ \text{diameter}^{\,2}}{4}\right. \\ &\quad \left. \cdot\ (\text{holes per board})(\text{array size})\right] \end{aligned} \quad (13)$$

where the smear thickness is the thickness of the layer coating the walls of the hole and, area is the area of the panel or board being processed. The total surface area of the holes is given by

$$\begin{aligned}\text{surface area}_{\text{holes}} &= \pi(\text{diameter})(\text{hole length}) \\ &\quad \cdot (\text{holes per board})(\text{array size}). \end{aligned} \quad (14)$$

The second term in (13) accounts for the fact that the desmear activity also etches surfaces besides the inside of holes [note, (plating thickness)(fraction etched) may be approximated by the smear thickness]. If a bath is used for desmearing, the volume of material wasted in the desmearing process is the sum of the etchant used [given by (3) with area replaced by the surface $\text{area}_{\text{holes}}$ from (14)]. If plasma desmear is used, (6) is used to compute the $\text{volume}_{\text{wasted}}$.

6) Filling: Several filling activities are supported in the present model: *fill holes*, *fill channels*, and *fill vias*. Filling is an important activity in some additive PWB fabrication approaches where conductors and/or vias are formed using photolithography techniques. Filling of mechanically drilled holes with paste or ink may be an activity in either conventional (subtractive) or in fully additive processes. The amount of material used to fill holes is given by

$$\text{volume}_{\text{used}} = (\text{hole length})(\text{area}_{\text{removed}}). \quad (15)$$

For drilled holes, hole length and $\text{area}_{\text{removed}}$ are computed during the drilling operation, (11) and (10). In the case of vias (that are assumed to extend only through the previous layer fabricated), the volume of material used for filling is given by (15) with the hole length replaced by the thickness of the last *plated*, *coated*, or *lamination* activity.

The volume of material used to fill the channels is

$$\begin{aligned}\text{volume}_{\text{used}} &= [(\text{area}_{\text{panel}})(\text{thickness})]\left[\frac{\text{LW}}{\text{LW + LS}}\ \text{wiring}_{\text{used}}\right] \\ &\quad \cdot \left[\frac{(\text{array size})(\text{area}_{\text{board}})}{(\text{area}_{\text{panel}})}\right] \end{aligned} \quad (16)$$

where

LW	line width (metal trace or channel) on the wiring layer;
LS	space between lines (metal traces or channels) on the wiring layer;
thickness	thickness of the last *plated, coated, or lamination activity*;
wiring_{used}	fraction of theoretically available wiring on the wiring layer that is actually needed for routhing.[2]

[2]In the context of (16), "route" refers to the process of wiring all the required electrical connections together as described by the netlist.

The first term in (16) is the pre-etch volume of the layer in which the channels are to be filled, the second term is the fraction of the layer that is actually channeled, and the third term is the fraction of the panel that is actually board area. The $\text{wiring}_{\text{used}}$ is determined from routing estimation methods that predict the total length of wiring necessary to route a specific design based on the number of components, the number of inputs and outputs (I/O), and the number of nets. See [11] for a summary of the methods used to predict application wiring requirements.

The second term in (16) assumes that all the wire widths and spacings on the layer are the same. In reality, wiring layers often use a variety of design rules; however, the approximation used in (16) is appropriate for system planning level analysis performed prior to layout and routing. The second term in (16) can be replaced by a more accurate estimation if one is available.

7) Singulation (*Fabrication, Routing*)*:* The process of singulating the boards from the panel is a major contributor to the waste stream. The fraction removed in the singulation activity is given by (9) where

$$\text{area}_{\text{removed}} = (\text{area}_{\text{panel}}) - (\text{area}_{\text{board}})(\text{array size}) \quad (17)$$

where array size is the number of boards per panel. As with drilling, the fraction removed is used to uniformly reduce the material used inventory and to add all of the material removed to the material waste inventory.

Equation (17) is used only when the board edge is homogeneous (i.e., every layer has the same area). If the board edge is not homogeneous the $\text{area}_{\text{removed}}$ must be computed separately for each layer.

8) Scrapping: In addition to having a significant impact on cost and quality, scrap is an important contributor to the waste stream. Test and inspection activities determine the fraction of individual boards or panels that are scrapped. When a panel or board is removed from the process flow (because it was either correctly or incorrectly found defective by a test or inspection step), all the money spent on it and all the materials associated with it (both the materials in the panel or board, and the waste materials associated with processing it to its present state) must be reallocated over all the panels or boards still in the process. The process that manipulates the inventories when parts are scrapped is shown in Fig. 2. The material used inventory is unaffected by scrapping, but the material wasted inventory is modified as

$$\begin{aligned}&\text{new inventory}_{\text{waste/board}} \\ &\quad = \left[(\text{inventory}_{\text{waste/board}}) + (\text{inventory}_{\text{used/board}})\right] \\ &\quad \cdot \left[\frac{\text{scrap}}{1 - \text{scrap}}\right] \end{aligned} \quad (18)$$

where scrap is the fraction of panels or boards removed from the process flow at a test or inspection step. The variable scrap is a function of the incoming yield_{in} (or $1 - \text{defectivity}_{\text{in}}$) of the parts and of the test coverage associated with the step [12]

$$\text{scrap} = 1 - (\text{yield}_{\text{in}})^{\text{test coverage}} \quad (19)$$

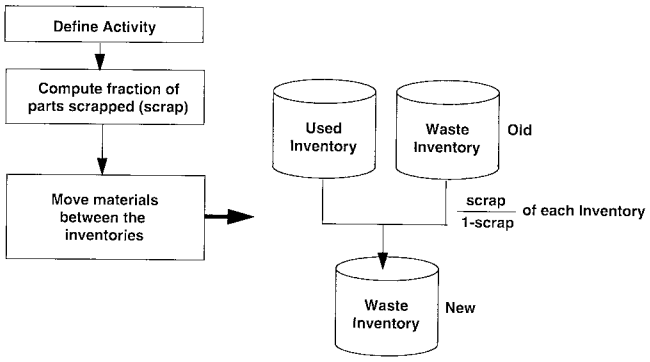

Fig. 2. Modeling process for defective parts that are scrapped as a result of inspection or test activities. scrap is the fraction of panels or boards scrapped by the test or inspection step.

where

$$\begin{aligned}\text{test coverage} &= 1 - \text{probability of not detecting a defect at test or inspection}\\ \text{yield}_{\text{in}} &= 1 - \text{defectivity}_{\text{in}}\\ \text{defectivity} &= \text{total fraction defective through product life (process + test + field failures)}\\ \text{defectivity}_{\text{in}} &= \text{fraction defective prior to a test or inspection step and subsequent scrap.}\end{aligned}$$

Equation (18) is complete only under the assumption that none of the defective parts can be repaired and reinserted into the process. If repair is possible, a more complex treatment is necessary [13].

Test and inspection steps can also involve any of the other material activities discussed in this section, including the use of consumables.

Note, the *scrapping* activity is the only material use or waste calculation that ever directly modifies the waste inventory (all others simply contribute to it).

9) Waste Disposition: There are no specific material volume calculations associated with waste disposition. The process that manipulates the inventories for waste disposition activities is shown in Fig. 3. At the simplest level, waste disposition costs are computed by extracting the volume of the specified waste from the waste inventory and multiplying it by the cost/volume of its treatment (note, the cost/volume can be negative if the waste can be sold, e.g., used drill bits). The only modification to the waste inventory that is necessary is to replace the processed waste material with a "remnant." A remnant is a version (or a portion) of the original waste material that is tagged to indicate that a waste disposition activity has been performed on it.

All the analyses discussed in this section assume that only one unique board design is fabricated on the panel. If the panel contains more than one unique board design, then, in general, the volume used and the associated waste computed per the equations in this section must be multiplied by the fraction of the panel used for the board design of interest. In cases where an array size (number of boards on the panel) appears in the relation, the effects of more than one board design on the panel can be used to modify the array size directly.

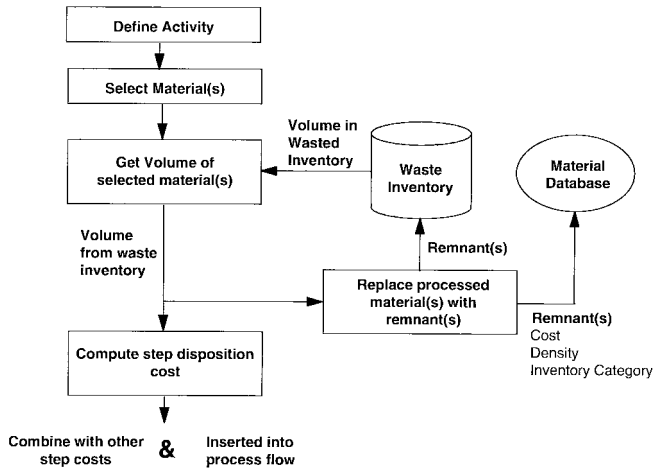

Fig. 3. Modeling process for treating disposition of wastes in the waste inventory. A "remnant" is a portion of the original waste material that is tagged to indicated that a waste disposition activity has been performed on it.

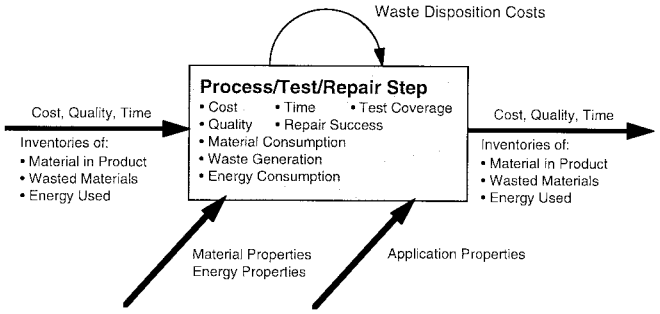

Fig. 4. General process step model used within the SavanSys software tool.

C. Model Implementation

On an individual process step basis, the material cost is computed by multiplying the $\text{volume}_{\text{used}}$ and/or $\text{volume}_{\text{wasted}}$ associated with the particular activity by the cost of the material. The material cost is then combined with the labor, allocated tooling, and allocated equipment costs to form the entire cost of the process step.

The modeling described in this paper was implemented within the SavanSys tradeoff analysis tool from Nu Thena Systems, Inc. [4]. The tool performs process flow modeling by providing a set of process step objects that may be combined by the user to describe a process flow. Process steps can be defined at a high level (cost, yield), or a detailed level (time, labor rates, material costs, equipment costs, tooling costs, etc.). Process flows can be constructed with a mixture of both types of steps. In addition to the material inventories, cost (recurring and nonrecurring), quality (defect density or yield), and time are accumulated through the process flow by the tool (Fig. 4).

When executed, each step in the process flow uses its local data to modify the cumulative cost, quality, and time associated with the object being manufactured. Process steps may be grouped and repeated. The number of repetitions is either specified by the user or referenced to a function of a product property (e.g., the number of wiring layers in a board divided by two). Processing may also occur in array formats or single objects, for example, a panel or single board could

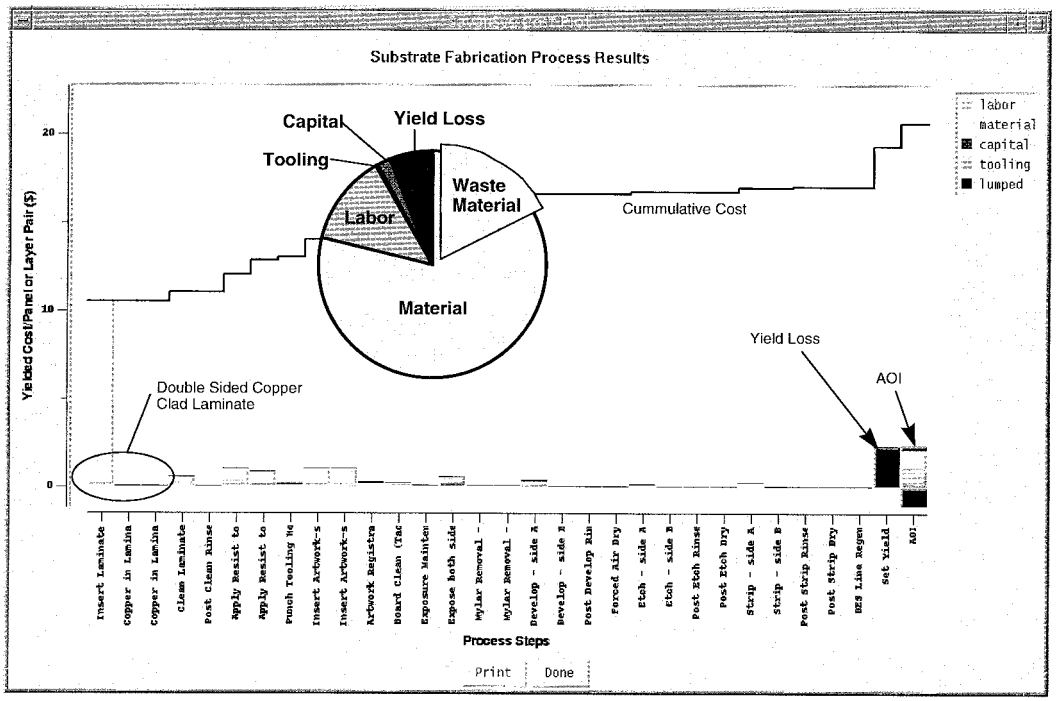

Fig. 5. Cost as a function of process step for the fabrication of a double-sided, undrilled, copper clad layer-pair. The embedded pie chart shows the fractional distribution of labor, material, tooling, and capital costs. The portion of the material cost that ends up being wasted is shown as a raised pie slice.

be processed. The tool automatically maps the cost and defect density of a panel to the cost and yield of a board when a format change is detected.

In addition to detailed cost analysis, the tool concurrently computes physical (size, weight, interconnect routing requirements, escape routing), electrical (delays, attenuation, dc drops, effective inductance), thermal (internal and external thermal resistances, air cooling), and reliability (MTTF) performance metrics for application specific multichip systems. SavanSys is integrated into the Mentor Graphics and Cadence physical design frameworks and is compatible with Aspect and DIE format databases.

III. An Illustrative Example

This section presents a simple illustrative example analysis performed using the model presented in Section II. All the results and figures in this section were automatically generated by the model discussed in Section II. An actual tradeoff analysis appears in Section IV of this paper. The analysis in this section is intended for demonstrative purposes.

The example presented here is the fabrication of a double-sided, undrilled, copper clad layer-pair for use in conventional PWB fabrication. The costs as a function of process step are shown in Fig. 5. The plot shows cost broken down by labor, material (computed using the methodology discussed in this paper), tooling, capital, and lumped. The "lumped" cost represents the effective cost of yield loss. The total cost of an 18 $\times$ 24 in layer-pair fabrication in this case is \$19.38 with a yield of 94% per layer-pair (yielded cost = \$20.62/layer-pair). Approximately half the cost of the layer-pair is the cost of the laminate inserted in the first step. Other significant contributors include the cost of resist (steps 6 and 7), artwork (steps 9 and 10), and the automatic optical inspection (AOI) step at the end of the process flow. The AOI step includes the cost of performing the inspection (labor and capital) plus the reallocation of money spent on layer-pairs that are scrapped by the AOI into the layer-pairs that are passed by the inspection. The pie chart included in Fig. 5 shows the relative contributions of labor, material, capital, tooling, and yield loss to the cost of a layer-pair. The pie chart also shows the fraction of the cost that has been invested in material that is wasted prior to completing the processing of the layer-pair. Note that the AOI step includes material in addition to labor and capital contributions. While the AOI activity has no direct material cost associated with it, the process involves scrapping layer-pairs that contain material investments. The material investments are allocated back into the layer-pairs passed by AOI; this reallocation is shown as a material cost associated with the AOI step. Waste disposition costs associated with the waste material from layer-pair fabrication is considered at the end of the full multilayer build (see Section IV).

The materials used for layer-pair fabrication are shown in Fig. 6. Nearly all the volume of material that is present in the final layer-pair is added by the copper clad laminate (first three steps). Application of the resist is shown in steps 6 and 7. The develop process removes all of the resist except that which covers the metal features desired on the layer. Etching removes all the copper that is not protected by the resist, and strip removes the remainder of the resist. There are other second order variations in the material usage that are too small to be seen in Fig. 6, such as a slight reduction in the volume of material in the layer-pair in the "Mylar Removal" steps in the middle of the flow. Mylar removal is the step where Mylar that is protecting the resist layers is removed and discarded.

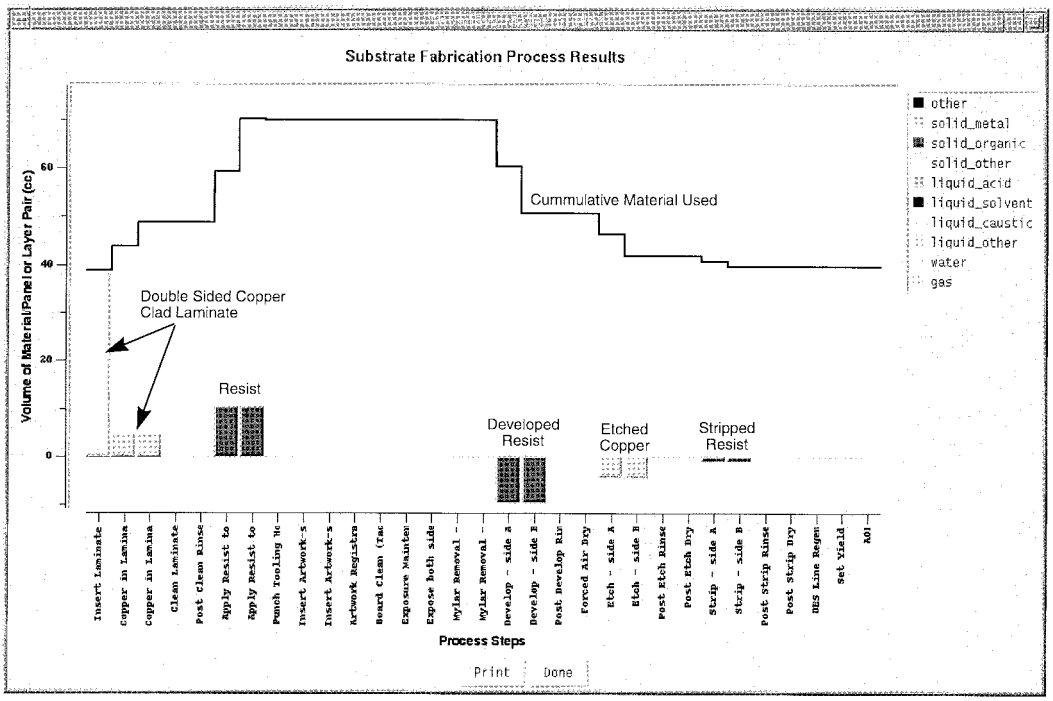

Fig. 6. Material used (material in the product) as a function of the process steps associated with fabricating a double-sided, undrilled, copper clad layer-pair.

Fig. 7 shows the material wasted as a function of process step in the layer-pair fabrication. Most of the waste generated is water from the rinse activities; however, nearly 1000 cc of nonwater waste is also produced. The nonwater waste is composed primarily of developer and stripper but also includes cleaners, resist, Mylar, and artwork. Note that the first three steps (the initial laminate insertion) produces no waste for the layer-pair fabrication. Obviously once the layer-pairs are used in the fabrication of an actual PWB, there will be considerable waste laminate generated when individual boards are singulated from the panel. That waste laminate will not be inserted into the waste inventory until the singulation activity occurs, i.e., all the laminate used to make the layer-pair is still part of the layer-pair at the end of this example. The AOI step at the end of the flow contributes significantly to the waste inventory because it scraps some of the layer-pairs that have been produced. All the materials in the scrapped layer-pairs *and* all the waste allocated to the scrapped layer-pairs must be reallocated into the waste inventory for the nonscrapped layer-pairs. Included in the waste that must be reallocated is the waste water used to produce the scrapped layer-pairs as well as the original laminate and resist used to produce the scrapped layer-pairs.

IV. A Comparison of Board Fabrication Technologies

In this section, we present the results of technology tradeoff analyses that compare PWB's fabricated using conventional mechanically drilled and plated through-holes and PWB's fabricated using photolithographically defined vias and conductive ink. The common driver behind all the fabrication variations considered in this section is reduction of the volume of waste resulting from the process, and thereby a reduction in the waste disposition costs. The first section compares alternative resists for fabricating conventional boards, while the second section compares the conventional board fabrication to the microvia constructions. Alternative cost comparisons of conventional and microvia board fabrication technologies have appeared in previous works [14] and [15]; however, no other studies to date consider the details of material usage, waste, and waste disposition that are treated here.

All of the analysis in this section is based on constructing four 6×9 in boards on an 18×24 in panel. The application considered is a smart I/O module for a U.S. Navy standard airborne computer that can be implemented using either an eight layer conventional board (5 mil lines and spaces, 13.8 mil diameter through-holes) or six layer photovia board (6 mil lines and spaces, 9 mil diameter vias).

The costs appearing in the following discussion have been "generalized" so as to not reflect any specific manufacturing facility and should be considered accurate for relative comparison rather than absolute magnitude. Experience indicates that random errors account for an uncertainty of $\pm$\$0.70/board in all the following cost predictions.

A. Waste Reduction Through the Use of Alternative Resists for Conventional PWB Manufacture

The objective of this analysis is to evaluate the impact on the environmental and economic metrics of a modified approach to conventional PWB fabrication. This approach makes use of a developmental product at DuPont known as Permanent Innerlayer Resist (PIR) [16]. When using PIR, the photoresist used in patterning of the internal layers is left on top of the copper circuits after develop and etch of the layer-pairs. This approximately 1-mil thick film acts as an

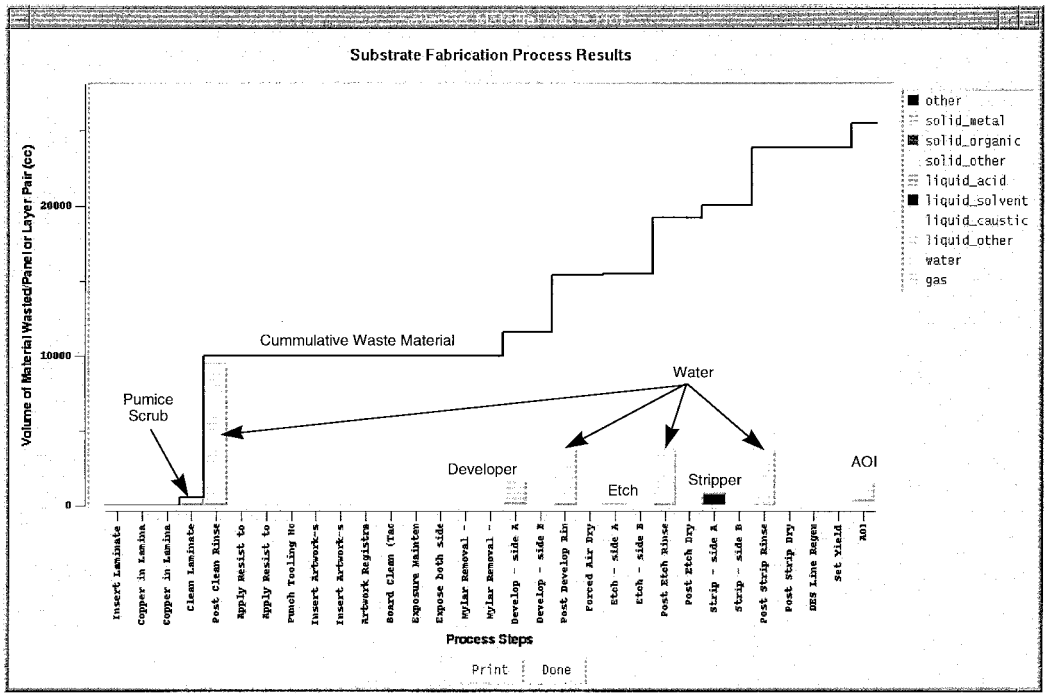

Fig. 7. Material wasted as a function of the process steps associated with fabricating a double-sided, undrilled, copper clad layer-pair.

adhesion promoter, a function typically achieved by oxidizing the copper traces. By using PIR, a board shop can eliminate the stripping and oxide treatment processes and associated waste streams, with consequent environmental benefit as well as reduction in production costs. Oxide treatment for improved Cu/prepreg adhesion is one of the dirtier processes in PWB fabrication. The strong caustic at high temperature required for the oxide process is costly to use and dispose of due to the high pH, oxidizers present, and dissolved metals built up over time. Elimination of the oxide process would also reduce water usage. In addition, use of PIR would eliminate stripping and its associated nonhazardous waste and water usage.

The biggest contributors to cost in the fabrication of a multilayer board, whether conventional or using PIR, are press lamination, fabrication of the layer-pairs, electrical test and inspection, and application of the solder mask to the outer layers. Material costs are the primary drivers for the layer-pairs and solder mask application, while labor and capital equipment are the primary cost drivers for electrical test and inspection.

A cost comparison of PIR with the conventional approach for layer-pair fabrication through oxidation is shown in Fig. 8. As can be seen by the graph, most of the cost for both approaches resides in the laminate (predominately material costs), followed by artwork, AOI (labor and equipment costs plus reallocated material costs from scrapped layer-pairs), and resist. There are five steps within the layer-pair construction at which the cost differs. The prebake and final cure steps are required only by the PIR approach, but their cost is minimal. The expose step for PIR has a slightly higher cost because PIR requires a higher exposure energy and therefore a slightly longer process time. These costs are offset, however, by the cost of strip and oxidation which are required for the conventional approach but not by the PIR approach.

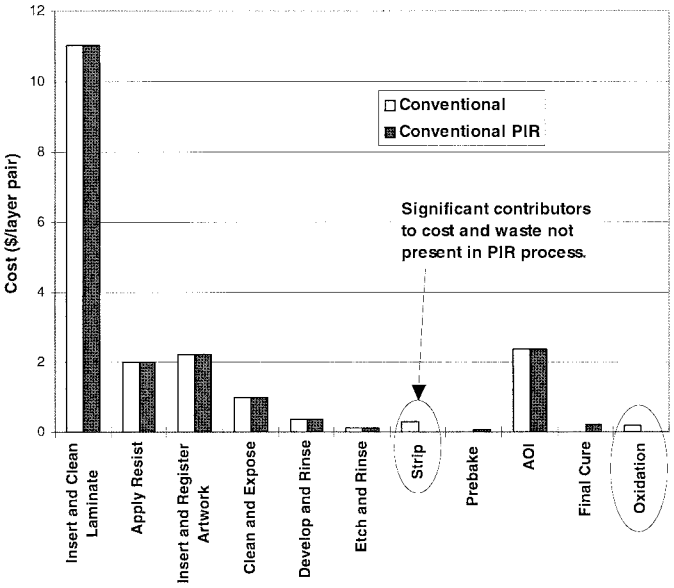

Fig. 8. Cost of conventional and PIR layer-pair fabrication including oxide treatment, excluding waste disposition. (The actual process models used consist of ~30 process steps that have been combined in this figure for convenience.)

The total cost for PIR is virtually identical to the cost of the conventional approach for the fabrication of layer-pairs. However, it should be noted that waste treatment costs are calculated at the end of the multilayer build, not stepwise through the process. If included at this point, the cost of the PIR approach through oxidation would be lower than the conventional approach.

Fig. 9 shows a cost comparison of PIR versus conventional processes for the entire multilayer build (eight layers). The

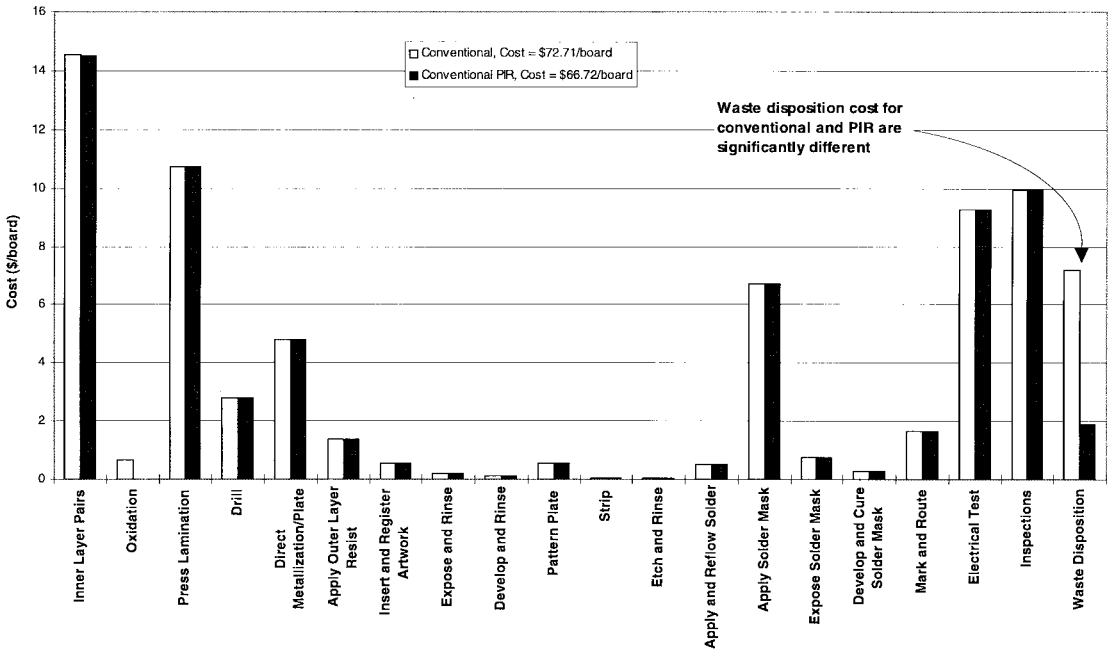

Fig. 9. Cost of conventional and PIR full multilayer build including waste disposition. (The actual process models used consist of ~230 process steps that have been combined in this figure of convenience.)

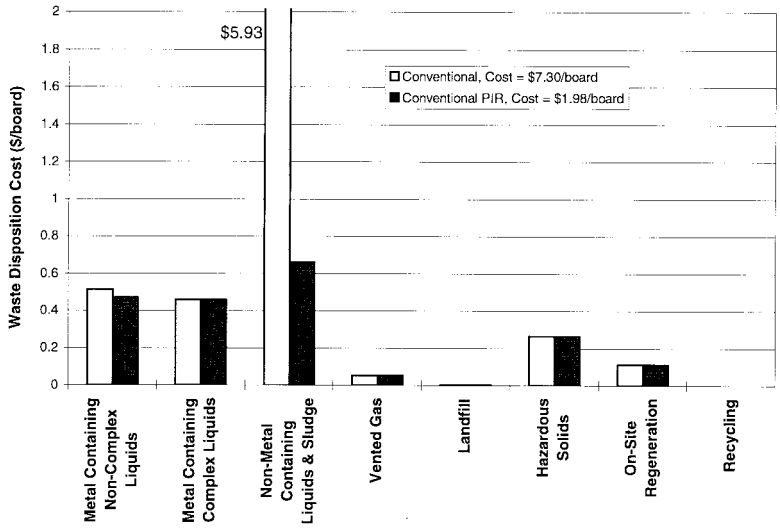

Fig. 10. Waste disposition costs as a function of material category. The "nonmetal containing liquids and sludge" category includes water.

primary cost differentiators are the oxidation process costs and increased waste treatment and extra disposal costs for conventional. The increased disposal cost for the conventional process is due to greater water usage associated with oxidation. A comparison of the total cost of a PIR and conventional multilayer build without considering the waste disposition indicates that the two approaches have virtually identical costs.

The impact of waste treatment costs for the conventional approach is striking. At over $7/board, this cost is more than three times that of the PIR approach, for which the waste treatment costs are just under $2/board. The primary driver is the amount of water required by the conventional process, which increases sewage and sludge disposition costs. This difference is seen in Fig. 10.

If the entire multilayer build for both conventional and PIR approaches is compared, the PIR process costs $66.72/board versus $72.71/board for the conventional process, a delta of $5.99 or a 8% reduction in cost. In summation, the additional process costs for PIR (cure and expose time) are offset by the cost of eliminating the strip and oxidation processes used in the conventional approach. The savings in waste treatment costs for the PIR approach, however, result in savings in overall board fabrication costs when compared to the conventional approach.

The PIR approach offers the potential of a nearly 8% cost savings for a multilayer board, with the primary cost benefit being in reduced water usage. Total waste was reduced from 427 liters of waste per board to 41 liters/board using PIR,

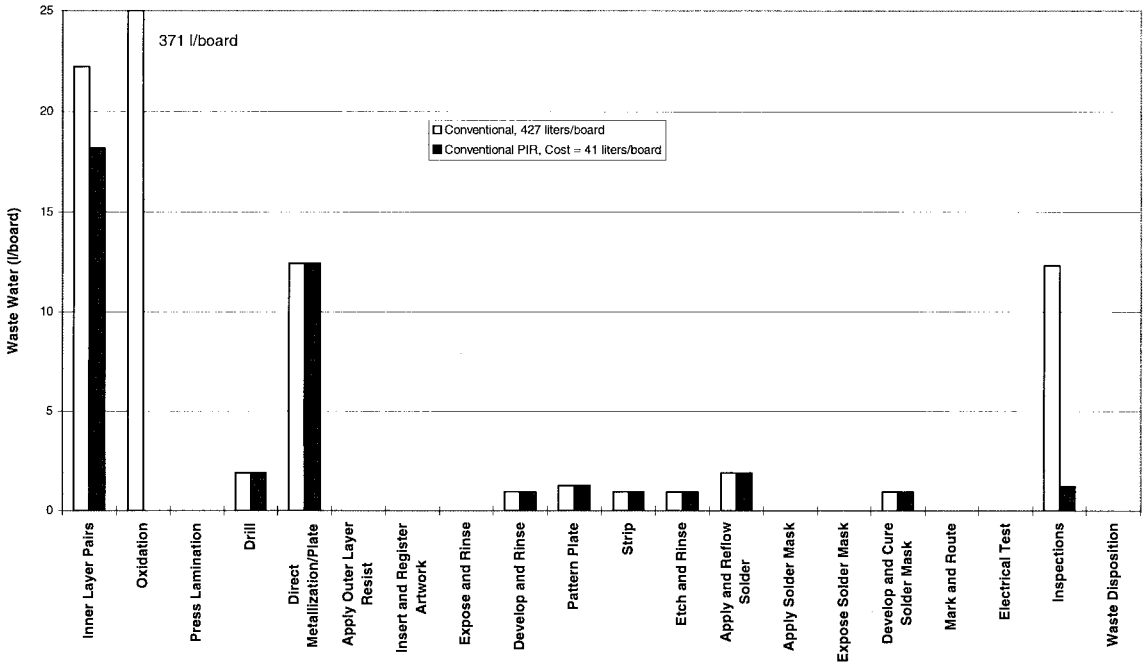

Fig. 11. Waste water of conventional and PIR full multilayer build. (The actual process models used consist of ∼230 process steps that have been combined in this figure of convenience.)

where most of the waste reduction was water, Fig. 11. Waste excluding water and gas was reduced from 5.3–3.8 liters/board (28%). There was no reduction in hazardous waste, as the only RCRA type-D hazardous material used in either process is the lead solder, which is not influenced by the PIR process.

B. Photovia versus Conventional PWB Fabrication

The objective of this analysis is to evaluate the economics of a fully-additive photovia approach to PWB fabrication. The photovia approaches make use of a developmental product at DuPont known as permanent dielectric dry film (PDDF) [17] and metallization using Ormet 3005 conductive ink from Ormet Corp., or Circuposit 71 (CP-71), a full build electroless copper process from Shipley. The construction of fully-additive boards begins with a dielectric core between 30 and 50 mils thick. Relatively large (>28 mil diameter) through-holes are drilled through the core substrate and filled with CB 100 conductive paste from DuPont. Signal layers and via layers are added sequentially to each side of the core using PDDF to form the pattern and provide electrical isolation. Full build electroless copper or conductive ink is added to the channels and via holes within the layers. Detailed descriptions of the photovia fabrication approaches appear in [17] and [18]. It should be stressed that the photovia results in this section assume a level of process maturity that is not available at this time; although operational boards have been fabricated using the process modeled here, they have been fabricated on smaller dimension panels in a prototype manufacturing environment. The panel size and quantities have been scaled upward for comparison purposes.

Fig. 12 shows a comparison of the process activity costs associated with the ink and electroless photovia fabrication approaches. Overall, the most significant cost contributor is the cost of the PDDF. The conductive ink approach is slightly less expensive than the electroless approach; however, we expect the difference to become more pronounced once conductive ink material costs decrease with maturity. Significant cost differentiators include filling the through-holes drilled in the core and waste disposition. In order to achieve an overall specified thickness for the board, the core substrate is thicker and consequently the through-holes are larger for the electroless build. As a result, this approach requires more conductive paste and more labor to fill the core vias than does the conductive ink approach.

The ink photovia approach uses less than half as much water as the electroless copper approach (19 versus 39 liters/board). The difference in water usage is due to the selective catalyzation process (swell, etch, and sensitization) required by the CP-71 electroless copper plating process (Fig. 13). Total waste for the ink process is approximately 39% less than for the electroless process (30 versus 50 liters/board).

Complete comparisons of board cost and waste disposition costs for the conventional and photovia processes are shown in Figs. 14 and 15. The comparison is for eight layer conventional boards and six layer photovia boards. Fig. 14 shows that although fabrication of the multilayer build (all processing up to the outer layer fabrication, excluding waste disposition) is significantly less expensive for conventional boards, the reduced expense of the photovia outer layer fabrication and waste disposition more than make up the difference. The photovia boards cost approximately 5–8% less than a conventional board for this application, although the conventional board with PIR resist gave the least expensive result at $66.72 per board. Total waste volume was reduced sharply due to reductions in the amount of water used. The conventional board generated 427 l/board of waste water while

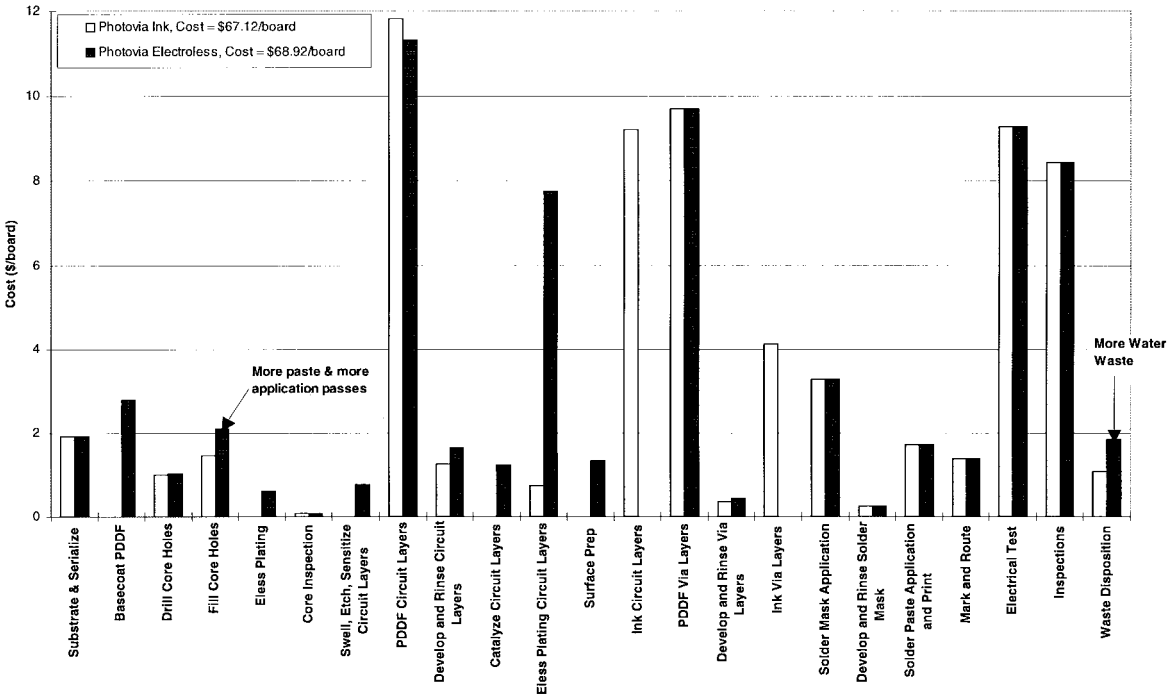

Fig. 12. Cost of ink and electroless metallization fully-additive photovia PWB fabrication processes including waste disposition. (The actual process models used consist of 250–350 process steps that have been combined in this figure of convenience.)

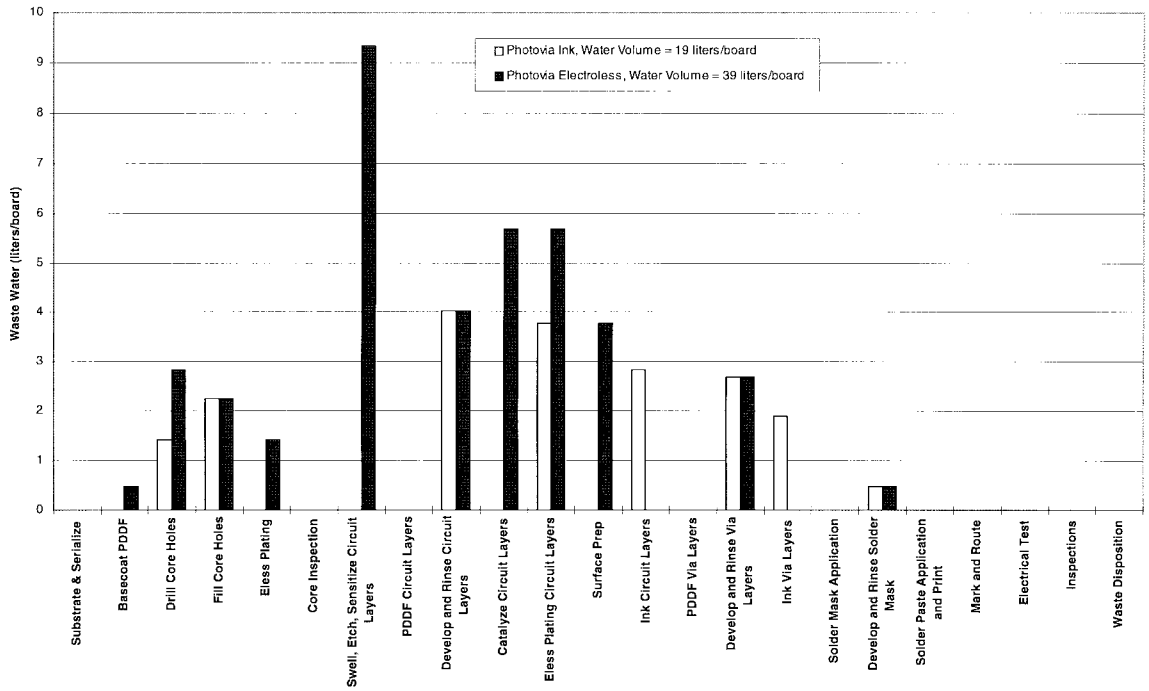

Fig. 13. Waste water of ink and electroless metallization fully-additive photovia PWB fabrication processes including waste disposition. (The actual process models used consist of 250–350 process steps that have been combined in this figure of convenience.)

the other builds gave: PIR—41 l/board, ink photovia—19 l/board, and electroless copper photovia—39 l/board.

V. Conclusion

In this paper, we have presented an activity-based cost model for PWB fabrication in which the process steps are defined by material processing activities. The model was applied to trading off the cost and waste associated with fabricating traditional mechanically drilled and plated through-hole PWB's with conventional and alternative resists and two variations of a fully-additive photolithographic microvia PWB fabrication process. Results of the tradeoff analysis for eight

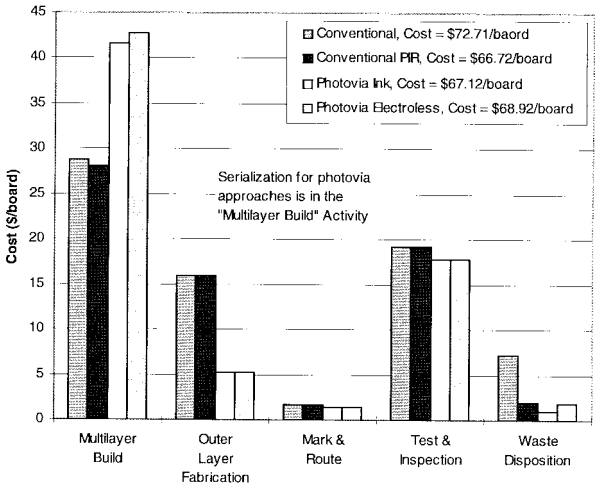

Fig. 14. Cost versus activity comparison of eight layer conventional board and six layer photovia board fabrication processes.

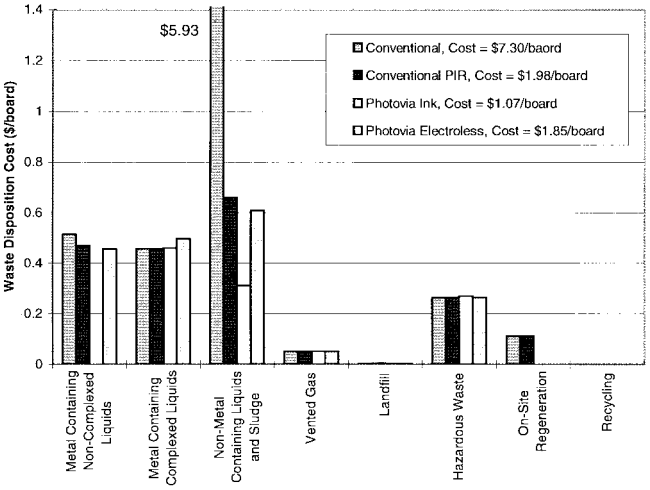

Fig. 15. Waste disposition cost versus activity comparison of 8 layer conventional board and 6 layer photovia board fabrication processes.

layer conventional and six layer photovia builds of four 6 × 9 in boards on an 18 × 24 in panel indicate the following:

1) Conventional board fabrication with PIR instead of conventional dry film photoresist reduces water usage by 10×, decreasing the overall board fabrication cost by 8%.
2) The conductive ink photovia build is slightly less expensive than the electroless copper build and uses half as much water.
3) Including waste disposition costs, a six layer photovia board is 5–8% less expensive than an eight layer conventional board build using conventional resists. A conventional eight layer board using PIR as the resist was the least expensive approach.

It should be stressed that these comparison result are application dependent, i.e., the relative conclusions could be different for other sizes of boards with different layer count ranges. It should also be emphasized that the photovia results in this paper assume a level of process maturity that is not available at this time.

Making the most appropriate tradeoff decisions to optimize a system requires an analysis treatment that is application specific and can capture fabrication cost details. The required tradeoff analysis including detailed cost prediction is possible and practical at the system planning phase of design using methodologies and tools like those presented here.

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REFERENCES

[1] D. L. Dance, T. DiFloria, and D. W. Jimenez, "Modeling the cost of ownership of assembly and inspection," *IEEE Trans. Comp., Packag., Manufact. Technol.*, vol. 19, pp. 57–60, Jan. 1996.
[2] "Environmental consciousness: A strategic competitiveness issue for the electronics and computer industry," Tech. Rep. CORP-064-93, Microelectronics and Computer Technology Corp., Austin, TX, 1993.
[3] *SEMI Compilation of Terms.* Mountain View, CA: Semiconductor Equipment and Materials International, 1995, p. 13.
[4] P. Sandborn, "Optimizing the design of high-density systems," *Electron. Packag. Prod.*, vol. 36, pp. 53–60, Sept. 1996.
[5] P. A. Sandborn and G. McFall, "Performing design for environment concurrent with interdisciplinary tradeoff analysis of electronic systems," in *Proc. IEEE Int. Symp. Electron. Environ.*, Dallas, TX, May 1996, pp. 167–172.
[6] S. Siddhaye and P. Sheng, "Integration of environmental factors in process modeling for printed circuit board manufacturing, Part II: fabrication," in *Proc. IEEE Int. Symp. Electron. Environ.*, San Francisco, CA, May 1997, pp. 226–233.
[7] C. Wilson, P. A. Sandborn, and G. Pitts, "Design-for-environment—A survey of current practices and tools," in *Proc. IEEE Int. Symp. Electron. Environ.*, Dallas, TX, May 1996, pp. 1–6.
[8] H. M. Karandikar, C. Kostas, and R. C. White, "Minimizing the environmental impact of printed circuit boards and assemblies through smarter design," in *Proc. Mentor Graphics Users Group*, Portland, OR, Oct. 1996.
[9] W. Lashbrook, P. O'Hara, D. Dance, and A. Veltri, "Design for environment tools for management decision making a selected case study," in *Proc. IEEE Int. Symp. Electron. Environ.*, San Francisco, CA, May 1997, pp. 99–104.
[10] P. A. Sandborn, J. W. Lott, and C. F. Murphy, "Material-centric process flow modeling of PWB fabrication and waste disposal," in *Proc. IPC Printed Circuits Expo*, San Jose, CA, 1997, pp. S10-4-4–S10-4-12.
[11] P. Sandborn and P. Spletter, "A comparison of routing estimation methods for microelectronic modules," in *Proc. Int. Electron. Packag. Conf.*, Austin, TX, Sept. 1996, pp. 651–663.
[12] T. W. Williams and N. C. Brown, "Defect level as a function of fault coverage," *IEEE Trans. Comput.*, vol. C-30, pp. 987–988, Dec. 1981.
[13] M. Abadir, A. Parikh, L. Bal, P. Sandborn, and C. Murphy, "High level test economics advisor (Hi-TEA)," *J. Electron. Testing*, vol. 5, pp. 195–206, 1994.
[14] H. Holden, "Comparing costs for various PWB build-up technologies," in *Proc. Int. Conf. Multichip Modules*, Denver, CO, 1996, pp. 15–21.
[15] A. Singer and R. Bhatkal, "A cost analysis of microvia technologies: Photo versus plasma versus laser," in *Proc. IPC Printed Circuits Expo*, San Jose, CA, 1997, pp. S17-4-1–S17-4-9.
[16] J. Lott, S. Quindlen, and D. Vaughan, "Environmentally conscious materials as part of DuPont electronic materials technology roadmap," in *Proc. IEEE Int. Symp. Electron. Environ.*, San Francisco, CA, 1997, pp. 234–239.
[17] J. W. Lott, R. K. Kraus, and C. F. Murphy, "High-density laminate substrates using a nonsubtractive manufacturing process," in *Proc. Int. Conf. Multichip Modules*, Denver, CO, 1997, pp. 75–80.

[18] C. F. Murphy, P. A. Sandborn, G. H. Schuldt, and J. W. Lott, "An environmental and economic comparison of additive and subtractive approaches for printed wiring board fabrication," in *Proc. IEEE Int. Symp. Electron. Environ.*, San Francisco, CA, 1997, pp. 240–245.

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