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Economic Analysis of Test Process Flows for Multichip Modules Using Known Good Die

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Abstract. The cost and quality of a multichip assembly is highly dependent upon the cost and quality of the incoming die. In the case of a bare die assembly, it is often highly desirable to use either Known Good Die (KGD) or die that have been burned-in and tested to the same level of quality and reliability as their packaged die equivalents. However, performing full bare die burn-in and test may not always be cost-effective. This paper examines the question of whether it is always necessary to use KGD to produce a cost-effective multichip module (MCM) of acceptable quality. A process-flow based cost model is used to compare the cost and quality of MCMs assembled with KGD to MCMs assembled with die that have received wafer-level test only. In addition to test effectiveness at the wafer, die, and module level, factors that are considered include die complexity (size and I/O), number of die per MCM, the cost of producing the KGD, and rework costs and effectiveness. The cost model captures inputs from wafer fabrication through MCM assembly and rework. Monte Carlo simulation is used to account for uncertainty in the input data. The resulting sensitivity analyses give final MCM cost and quality as a function of the various factors for both KGD and die that have received wafer-level test only.

Keywords: multichip modules, known good die, bare die test

1. Introduction

The economic risks of producing bare die multichip assemblies, especially as a function of number of die per assembly and incoming die quality, are well documented [1–4]. The growth of the multichip module (MCM) industry to date has been hindered by concerns over the lack of availability and high cost of known good die (KGD). The ability to provide bare die that are known to be good, i.e., equivalent in quality to conventionally packaged parts, has spawned a new technology within the microelectronics industry, with more than 20 U.S. companies currently developing and/or providing single die carriers for burn-in and test. A complete discussion and analysis of these various technologies is given in [5].

Despite the level of effort currently being expended towards finding a solution to bare die-level burn-in and test, there are semiconductor manufacturers selling what are referred to as KGD that have not been burned-in, but which have high yields coming out of wafer-level test, either because of improved wafer testing techniques and/or statistical high grading (e.g., Lot Acceptance Testing). Other companies manufacture MCMs using die straight out of conventional wafer test. Typically in these cases, the die are relatively small, and the company has determined that it is less expensive to rework and/or scrap the multichip assembly than it is to burn-in and test individual bare die. These two scenarios raise the question: are KGD necessary in order to build cost-effective MCMs at an acceptable quality level?

This paper will examine the effects on final MCM cost and quality using a process flow based economic model. Modules assembled with KGD (i.e., those which have received die-level burn-in and test) are compared with equivalent modules assembled with die that have received wafer-level test (WLT) only. Cost and quality are examined as a function of wafer-level test effectiveness, die complexity (size and I/O), cost of KGD, number of die per MCM, and other factors. The reader is cautioned that the results presented here are meant to indicate trends and relative effects; absolute answers will differ depending on specific circumstances.

The purpose of the modeling effort and analysis presented here is to broadly address the economic and quality drivers for fully tested bare die. The results are first order estimations that are intended to give guidance to die suppliers as to when it is beneficial to perform the potentially costly and time-consuming task of bare die burn-in and test and to users of bare die as to when it is beneficial to pay for KGD. The results are not meant to be highly quantitative, although given specific inputs, the model itself is capable of producing more precise output. The inputs used are generalized and represent typical CMOS microprocessors and DRAMs of mid-range performance. These were selected because the major semiconductor houses are focusing their efforts on these product types for development of KGD technologies.

2. Methodology

Cost modeling of known good die has been discussed in previous works [5, 6] where the process flow was limited to wafer fabrication through single die burn-in and test. Analyses were concerned primarily with the cost of bare KGD relative to conventional packaged die. For this paper, the model has been modified to include assembly, test, and rework of the module. The approach is loosely based on the Hi-TEA model [7, 8] which is currently supported in a commercially available software tool from Savantage.

The cost model used in this paper is divided into nine steps, as shown in Table 1. Each step relies on several key input parameters; the most critical of the approximately 100 parameters are listed. Some of these parameters are external inputs that are entered by the operator of the model (e.g., die area and number of die per module), while others are computed based on the inputs generated within the model (e.g., defectivity of die on the wafer or die cost prior to MCM assembly). The user can also override the values of the computed parameters by directly supplying a value.

Table 1. Cost model process flow and key inputs.

Process step	Key parameters
Wafer fabrication	Die area, Number of I/O, Defects per unit area
Wafer-level test	Number of gates, Test coverage (effectiveness), Defectivity of incoming die (true wafer yield)
Assembly into a KGD carrier	Material costs (including KGD carrier), Number of uses per carrier, Equipment cost, Labor rates, Time per operation
Burn-in	Burn-in time, Burn-in costs, Operation parameters
Final test	Number of gates, Test coverage, Defectivity of incoming die
Disassembly from KGD carrier	Equipment cost, Labor rates, Time per operation, Reclaim costs
MCM assembly	Cost and quality of incoming materials (die and substrate), Number of die per module, Assembly costs, Assembly yield
MCM test	Number of die per module, Number of gates, Test coverage, Defectivity of incoming module
Rework	Cost of rework (including diagnosis, die removal, re-assembly and re-test), Defectivity of replacement die, Assembly yield, Rework yield, Diagnostic success

The model calculates the cumulative cost per die, or per MCM at the end of each process step using:

$$C_{\text{cum}} = \frac{C_n + \Sigma C_{(1,n-1)}}{\%\ \text{pass}_n} \quad (1)$$

C_{cum} Total cost to produce a single die or MCM from process steps 1 through n, adjusted to include the cost of producing scrapped material.

C_n Cost to process a single die or MCM at the current process step

$\Sigma C_{(1,n-1)}$ Total cost to produce a single die or MCM prior to the current process step

$\%\ \text{pass}_n$ Percent of the die or MCMs which pass the current process step and continue on to the next process step (i.e., percent not scrapped).

$P(zd)_{\text{cum}}$, or the probability that a die or MCM is defect free after a particular step n, is equal to one minus the probability that a defect has been introduced at any of the preceding process steps times the probability of introducing a defect at the current step. This assumes that there is no screening for defects (test or inspection) at this process step. A defect is defined as anything that will affect the functionality of the die or MCM over the lifetime of the product.

$$P(zd)_{\text{cum}_n} = 1 - (P(d)_{n-1} * P(d)_n) \quad (2)$$

$P(zd)_{\text{cum}_n}$ Probability of having zero defects on a die or MCM after completion of process steps 1 through n

$P(d)_{n-1}$ Probability of having a defect on a die or MCM after completion of process step $n-1$

$P(d)_n$ Probability of introducing defect on a die or MCM at process step n.

Within a single process step there may be multiple opportunities for introducing a defect. For example, at an assembly step defectivity is calculated as the probability of introducing a defect on a single bond site raised to the power of the number of bond sites.

$$P(\text{defective die})_n = P(\text{defective die})_{n-1} * P(\text{defective bond site})_n^{(\#\text{bond sites})}$$

The defectivities used in performing the analysis presented in this paper were derived from interviews with engineers working in large U.S. manufacturing companies. It was assumed that the processes and products were of average maturity. The defectivity of a die after completing wafer fabrication is calculated as a function of the total area of the die and the estimated defects per unit area for an established CMOS line [9].

The $\%\ \text{pass}_n$ at process steps that have no inspection or test associated with them is assumed, for the purpose of this modeling effort, to be 100%. At process steps where the primary purpose is to screen out defects (inspection or test steps), there are four possible scenarios: bad product is scrapped, good product is passed on to the next step, bad product is passed on to the next step, or good product is scrapped. This model accounts for only the first three (i.e., appropriately dispositioned good or bad product and escapes). It is also assumed that the probability of introducing defects at a test or inspection step is zero.

The $\%\ \text{pass}_n$ at a test or inspection process steps is estimated by:

$$\%\ \text{pass}_n = P(zd)_{n-1}^{P(\text{detection})_n} \quad (3)$$

$P(zd)_{n-1}$ Probability that there are no defects on the die or MCM upon entering the test or inspection step

P(detection)_n Probability that an existing defect will be detected at the current process step (i.e., $1 - \%$ escapes).

$P(\text{no defects})_n$, or the probability that a die or MCM is defect free after a test or inspection step n is estimated by:

$$P(zd)_{\text{cum}_n} = P(\text{no defects})_{n-1}^{(1-\text{P(detection)}_n)} \quad (4)$$

The probabilistic relationships expressed in Eqs. (3) and (4) are useful in more complex test coverage estimations as well (10, 11). The most difficult task is correctly estimating the probability of detecting a defect at test or inspection. In keeping with the language of prior works, the probability of detection will be referred to as "test coverage" throughout the remainder of this paper. This term is meant to denote a generic screening efficiency rather than the more specific meaning applied by test professionals.

The model contains approximately 100 input parameters. In our analysis, roughly half of these parameters were fixed at a single value while the remainder were defined as distributions. Distributed inputs permit the use of Monte Carlo simulation in the analysis. This

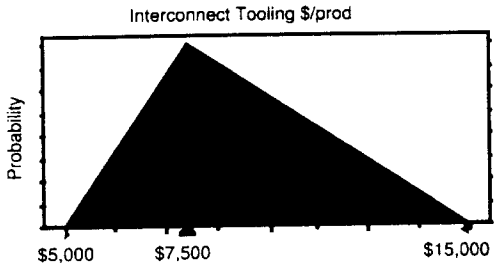

Fig. 1. Example of an input distribution.

is especially valuable for the die-level burn-in and test portion of the model, where there are a large number of inputs and a large amount of uncertainty. This is due primarily to the immaturity of the KGD carrier portion of the industry and a desire not to use values specific to a particular vendor's technology in the analysis. An example of a distributed input with a triangular distribution is given in Fig. 1, where the range for interconnect tooling is set at $5,000 to $15,000, with the most likely value being $8,000. Most of the inputs that represent multiple populations were modeled with triangular distributions, while inputs that belong to a single population were modeled by normal distributions.

A simplified approach was taken in order to explore the relative effects on the cost of multichip assemblies using incoming bare die. For the purpose of illustration and analysis, the assemblies are assumed to have all identical die. This is intended to simulate the situation where a bank of identical die (e.g., memories) are used in an MCM assembly. The model assumes an early KGD and MCM production environment with a die volume of 500,000 die starts.

A small number of the fixed inputs are used for sensitivity analyses. The initial set was chosen based on whether the factors are of particular interest or if it is anticipated that they will have a significant effect. The inputs are examined over predetermined ranges. As in any sensitivity analysis, the results are highly dependent upon the selection of the range, as this will affect the slope. The ranges presented here are based on industry inputs and may not be valid for the individual case.

Analysis tools such as ANOVA (analysis of variance) are used to evaluate the relative effects of the factors and to narrow down the number of variables of interest for further analysis. The selected ranges are not intended to be all encompassing and results can vary significantly depending upon the exact values selected as the end points. It is also important to note that since these are sensitivity analyses, the results point to the most critical factors for controlling cost and quality, which are not necessarily the single largest contributor to the MCM cost (or quality).

For example, assume that the cost of a substrate for a given MCM ranges from $50 to $60 on an approximately $100 module. The substrate is a significant cost contributor, constituting 50 to 60% of the total cost; however, at either extreme of the substrate cost range, the cost of the MCM will vary by only 10%. In contrast, assume the cost of each incoming die ranges from $1 to $5 (perhaps as a function of quality). On a 10 die MCM, this can result in a 40% variation in the total MCM cost ($100 vs. $140). Therefore, even though the die contribute less than 50% to the total MCM cost, variations in this factor have a much more significant effect than substrate cost.

A list of the factors used, along with their ranges, is given in Table 2. An explanation of each term and a discussion of the selected ranges for the various factors follows.

Die Complexity is a semi-quantitative factor. It is used to capture two of many die features which affect defectivity, test time, cost to fabricate, etc. This factor is most useful when used with in a product family, but also captures in a general sense the trends that result even when comparing across families. As stated previously, the purpose of this analysis is to provide guidance rather than specific data points. The range for die size and number of I/O is intended to be representative of the type of die which might be used in banks of identical die. Die complexity is calculated as:

$$\text{Die Complexity} = \text{Die Area (cm)} \times \log\ (\#\text{ of I/O}) \tag{5}$$

KGD Cost is the cost of performing burn-in and test on bare die using a single die carrier. The goal is to achieve the same level of quality and reliability as its packaged die equivalent. Cost increases as the burn-in cycle time increases and as product life time (i.e., time between re-designs) decreases. These factors were found to have the greatest influence on the cost of multiple-use single-die carriers [6], largely because they affect the number of uses over which the cost of the carrier can be amortized. The burn-in times selected are representative of commercial products. Military products would have much longer burn-in times which would significantly increase the cost of producing KGD. The KGD cost range used in

Table 2. Factors used in regression analysis.

Factor	Low	Medium	High
Die complexity	0.25 cm^2 (0.5 cm on a side) with 20 I/O	0.5 cm^2 (0.7 cm on a side) with 60 I/O	1.0 cm^2 (1.0 cm on a side) with 60 I/O
KGD cost	6 hr burn-in cycle 2 year product life	24 hr burn-in cycle 1 year product life	48 hr burn-in cycle 0.5 year product life
% Test coverage at Wafer test*	80%	90%	99%
%Test coverage at final test	98%	99%	99.99%
Die per Multichip assembly	4	10	15
Incoming substrate quality	98%	99%	99.9%
Assembly cost	$0.005 per pin $0.50 per cm (die) $2.50 per board	$0.01 per pin $1.00 per cm (die) $5.00 per board	$0.015 per pin $1.50 per cm (die) $7.50 per board
Assembly yield loss (per pin)	50 ppm (99.995%)	100 ppm (99.99%)	200 ppm (99.98%)
Diagnostic capability per die	95%	97%	99%
% Test coverage at Module test	90%	95%	99%

*Entered separately for KGD cases (die-level burn-in and test) and non-KGD cases (wafer-level test only).

this analysis, therefore, is probably most applicable to commercial products.

% *Test Coverage at Wafer Test* is a measure of screening efficiency at the wafer level and is simply the probability of detecting a defect at wafer test. It is intended to be a statistical expression that involves, but is not limited to, the traditional use of the term test coverage in test engineering. Wafer testing typically confirms and measures electrical viability rather than design functionality and is rarely done at speed. For the purpose of this analysis, wafer test is assumed to be statistically independent from other test steps.

% *Test Coverage at Final Test* is a measure of screening efficiency at the die level. As in the case of wafer test above, it is simply the probability of detecting a defect at die-level test. Final test is a functional test done at speed on either packaged die or bare die placed in temporary carriers. It typically has very high test coverage (in the traditional sense of the term) and therefore is expected to be much more efficient in detecting defects than wafer-level test. Consequently, a much higher statistical test coverage is assumed. However, we recognize that there may be many products for which this number is significantly lower. For the purpose of this analysis, final test is assumed to be statistically independent from other test steps.

Die per Multichip Assembly is a the number of die attached to the MCM substrate using wire-bond attach.

Incoming substrate quality is the probability of zero defects on an unpopulated MCM board as it enters the assembly line. In this analysis, this range may err on the high side.

Assembly cost is the cost of attaching the die to the substrate and wire-bonding each bond site. The selected cost range may be higher for more demanding product than what is assumed here.

Assembly yield loss (per pin) is the probability of creating a defective bond site.

Diagnostic capability per die is the ability to correctly locate a defective die site; the value is expressed per die. The die site may be defective due to a defective die, an assembly defect, or a board defect. The effects are estimated to be multiplicative and are intended to be only a rough estimate which will drive the model in the right direction. In the case

of a 95% diagnostic capability and 4 die per MCM, the probability of correctly locating a defect die site the first time is $.95^4$ or 81%. In the case of 15 die per MCM, the probability drops to 46%. These are not highly defensible numbers but the relative effect of increased difficulty in detection as a function of die per module is captured. It has been suggested that with constantly improving diagnostic capabilities, that the estimates used in this analysis may be lower than what actually can be achieved.

% *Test Coverage at Module Test* is a measure of screening efficiency at the module level . As in the case of wafer test and final test above, it is simply the probability of detecting a defect at MCM-level test. For the purpose of this analysis, module test is assumed to be statistically independent from other test steps.

3. Results of ANOVA

3.1. Overview

Analysis of variance (ANOVA), in combination with Monte Carlo simulation, was used to determine the relative importance of each of the factors listed in Table 2. Variables were ranked based on their ability to change the cost and/or quality of the outgoing MCM. The model simultaneously calculates the cost and quality of an MCM built with KGD or with die that have received wafer-level testing only. Results are included for 0 to 3 reworks. Also determined are the cost and quality ratios for an MCM assembled with KGD vs. one assembled with die which have received wafer-level test (WLT) only.

Table 3 and Fig. 2 indicate that the most significant effects on MCM cost, for MCMs assembled with KGD, are the number of die per MCM and die complexity (area and number of I/O). Both of these factors affect MCM cost by affecting the cost of the incoming die set and are critical with or without rework; however, both effects are greater in the case where rework is used. Rework has a significant effect because it allows for more efficient use of materials and labor (only the defective portions of the module are scrapped). This increases the relative effect of the single largest cost contributor, which is incoming die. Secondary effects on the total cost of the outgoing MCM are the cost of producing known good die (die-level burn-in and

Table 3. Factors affecting outgoing cost and quality of an MCM assembled with Known Good Die (KGD).

	Range of analysis		Total MCM cost relative effect		Outgoing MCM quality relative effect	
Factor	Low	High	No rework	3 reworks	No rework	3 reworks
Die complexity	0.25 cm^2 20 I/O	1.0 cm^2 160 I/O	High	High	High	High
KGD cost	2 year life 6 hr Burn-in	6 month life 48 hr Burn-in	Medium	Medium	—	—
% Test coverage at Wafer-level test	80%	99%	—	—	—	—
% Test coverage at Die-level test	98%	99.99%	—	—	Low	Low
Die per Multichip assembly	4	15	Very high	Very high	Medium	High
Incoming substrate quality	98%	99.9%	—	—	—	—
Assembly cost	$0.005 per pin, $0.50 per die cm $2.50 per board	$0.015 per pin, $1.50 per die cm $7.50 per board	Low	Low	—	—
Assembly yield loss (per pin)	50 ppm	200 ppm	Low	—	Medium	Medium
Diagnostic capability per die	95%	99%	—	—	—	Medium
%Test coverage at Module test	90%	99%	Medium	Medium	High	High

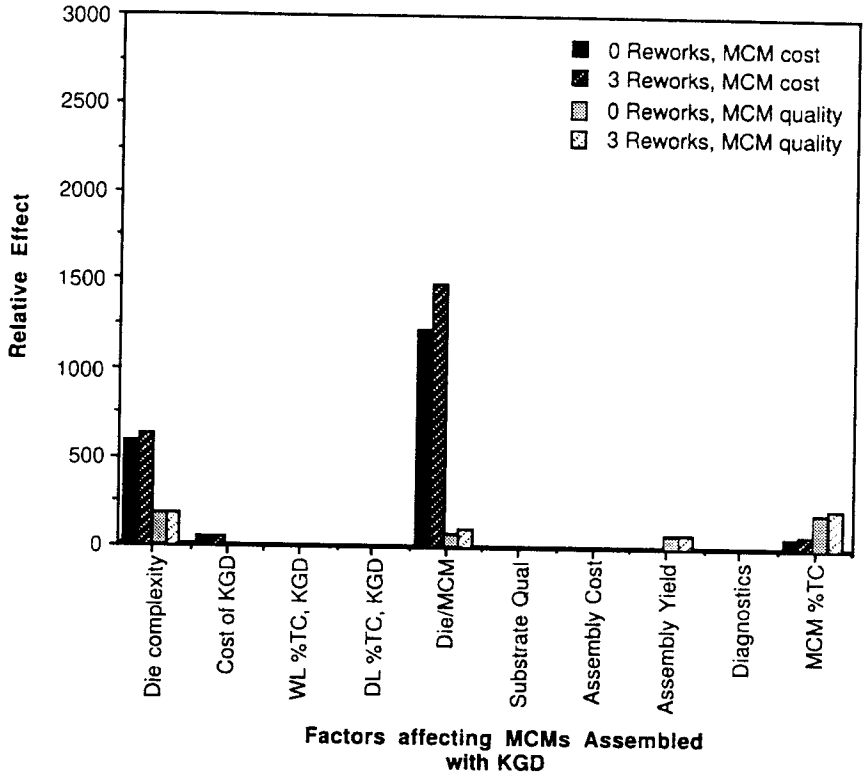

Fig. 2. Relative effects for MCMs assembled with KGD.

test) and MCM test coverage. The former increases incoming die costs and the latter results in increased scrap, to the benefit of outgoing quality.

MCM outgoing quality is determined by die complexity and the test coverage at MCM test. The more complex the die, the more likely the die are to have defects (even after test). Increased test coverage increases the outgoing die quality (Eq. (4)). Die per MCM and assembly yield also have some effects on the MCM outgoing quality.

MCMs assembled with die that have received wafer-level test only (WLT) are most significantly affected by die per assembly and die complexity (Table 4 and Fig. 3). Test coverage at the module level is also important in determining both final cost and quality. This is similar to the findings for MCMs assembled with KGD. A notable difference, however, is the effect of test coverage at the wafer level. In the case of MCMs assembled with KGD, test coverage at the wafer level (within the defined range) has no significant effect on either cost or quality; this is due to subsequent testing at die level. In contrast, both cost and quality of MCMs assembled with WLT are highly dependent on the level of screening at wafer level.

Interestingly, for the case of MCMs assembled with KGD, the analysis shows that die-level test coverage has only a small effect on quality and no statistically significant effect on cost. While this may seem counterintuitive, it is believed to be the result of several effects. First, the range of possible die-level test coverages evaluated is rather small: 98% to 99.99% for die level vs. 80% to 99% for wafer-level test coverage. In the case where die-level test is much more challenging this effect would be expected to be much larger. Secondly, the range in die size considered in this analysis is not particularly large and consequently yields are relatively high; it is likely that die-level test coverage would have a greater effect if larger die (with correspondingly lower yields) were considered. However, since increases in the cost of producing KGD are always offset by savings in scrap, the effect may be small for the majority of cases.

The discussions above apply to situations where the decision has already been made to assemble the module using either KGD or WLT. Within each of those systems, the factors will have the effects described. However, if the goal is to select the lower cost or higher quality approach, it is important to understand which

Table 4. Factors affecting outgoing cost and quality of an MCM assembled with Known Good Die (KGD).

	Range of analysis		Total MCM cost		Outgoing MCM quality	
Factor	Low	High	No rework	3 reworks	No rework	3 reworks
Die complexity	0.25 cm^2 20 I/O	1.0 cm^2 160 I/O	High	High	High	Medium
% Test coverage at Wafer-level test	80%	99%	Medium	Low	High	High
Die per Multichip assembly	4	15	High	Very high	High	Medium
Incoming substrate quality	98%	99.9%	—	—	—	—
Assembly cost	\$0.005 per pin, \$0.50 per die cm \$2.50 per board	\$0.015 per pin, \$1.50 per die cm \$7.50 per board	—	Low	—	—
Assembly yield loss (per pin)	50 ppm	200 ppm	—	—	—	—
Diagnostic capability per die	95%	99%	—	Low	—	Medium
%Test coverage at Module test	90%	99%	Medium	High	High	High

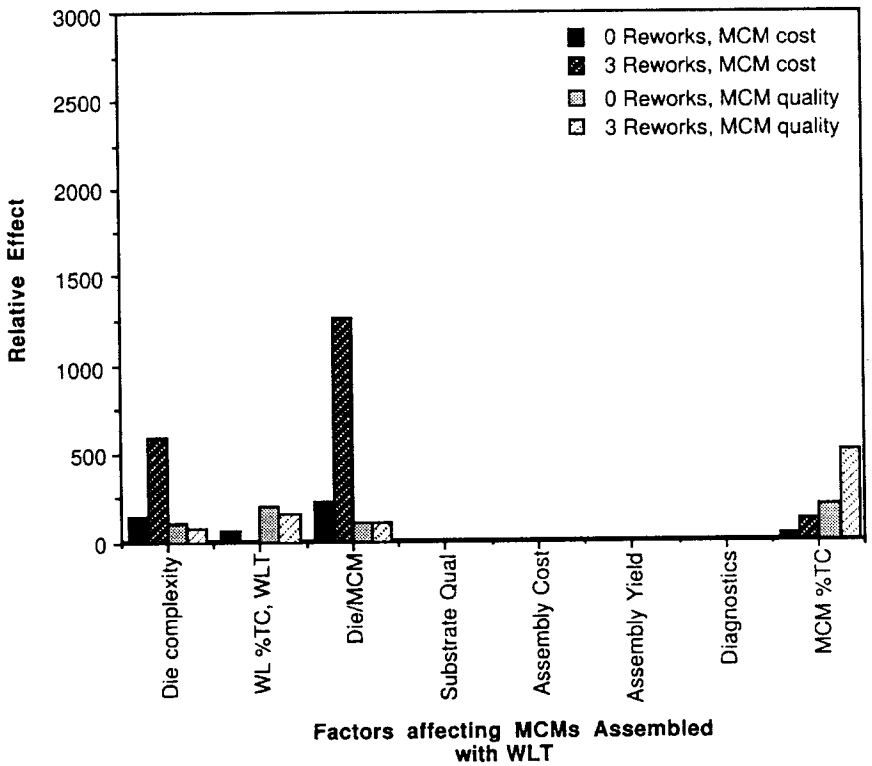

Fig. 3. Relative effects for MCMs assembled with WLT die.

Table 5. Factors affecting outgoing cost and quality of an MCM assembled with either KGD or WLT.

	Range of analysis		Total MCM cost		Outgoing MCM quality	
Factor	Low	High	No rework	3 reworks	No rework	3 reworks
Die complexity	0.25 cm^2 20 I/O	1.0 cm^2 160 I/O	High	High	Medium	Medium
KGD cost	2 year life 6 hr Burn-in	6 month life 48 hr Burn-in	Medium	High	—	—
% Test coverage at Wafer-level test,KGD	80%	99%	—	—	—	—
% Test coverage at Wafer-level test,WLT	80%	99%	High	High	High	High
% Test coverage at Die-level test,	98%	99.99%	—	—	—	—
Die per Multichip assembly	4	15	High	Medium	Medium	Medium
Incoming substrate quality	98%	99.9%	—	—	—	—
Assembly cost	$0.005 per pin, $0.50 per die cm $2.50 per board	$0.015 per pin, $1.50 per die cm $7.50 per board	—	—	—	—
Assembly yield loss (per pin)	50 ppm	200 ppm	—	—	—	Low
Diagnostic capability per die	95%	99%	—	Medium	—	Medium
%Test coverage at Module test	90%	99%	Medium	High	High	High

factors act as key drivers in determining whether KGD or WLT is the better choice, either in terms of cost or quality. Table 5 and Fig. 4 illustrate the effects of the various factors on two ratios:

1) MCM cost using KGD divided by MCM cost using WLT (KGD/WLT). When this value is greater than one, the KGD approach is the more costly, (i.e., less cost-effective) approach.
2) MCM quality using KGD divided by MCM quality using WLT (KGD/WLT). When this value is greater than one, the KGD approach is the higher quality approach.

The decision to use KGD or WLT in a given MCM assembly depends first upon whether rework is available or not. If rework is unavailable, then the key factor in determining whether KGD or WLT is the most cost-effective is the amount of test coverage available at wafer test for the WLT die. In the case where rework is available, however, the cost of producing KGD is the most important and the effect of wafer-level test coverage for WLT is roughly equivalent to the effects of die complexity and the amount of test coverage at MCM test. The quality ratio is dependent upon wafer-level test coverage for WLT and MCM test coverage. If rework is unavailable, the former is more important; if rework is available then MCM test coverage is the more important factor.

All of the quality numbers used in this analysis represent the defects present as the module is shipped. Latent defects, which are presumably screened out at burn-in, are not included. Therefore, for an equivalent quality value (KGD/WLT = 1), the KGD MCM will actually be of higher quality. Depending on the burn-in fall-out rate and its correlation to actual field failures, this difference may be very small or quite large.

Sensitivity analyses of the key factors were performed and are presented below. The analyses are run by setting the factor(s) of interest at fixed values within the range defined in Table 2; all other values are held at the mid-points. In the figures, open symbols with solid

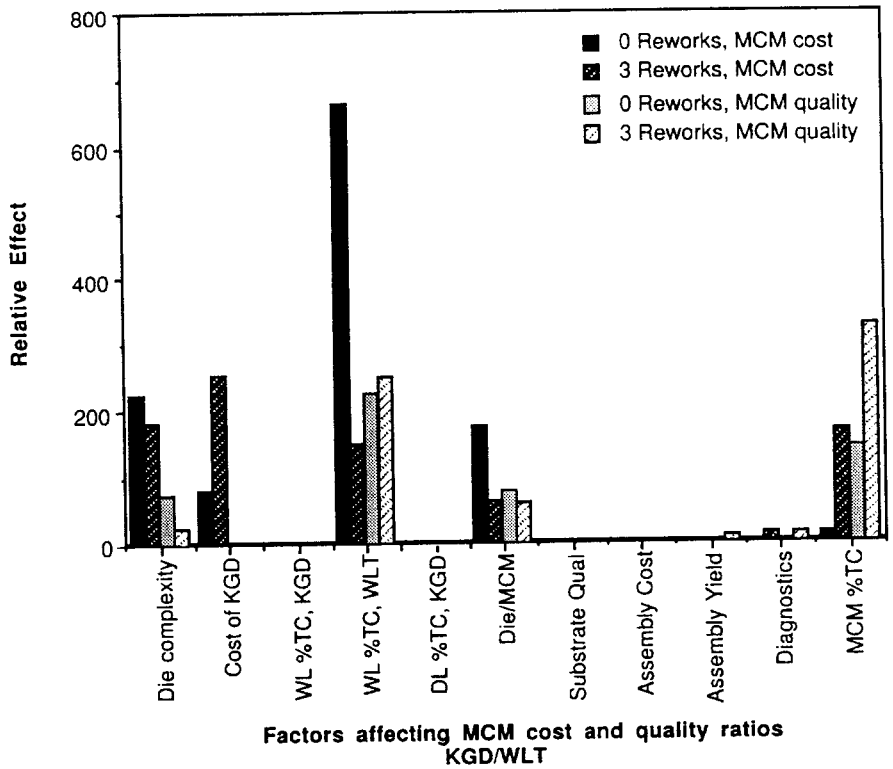

Fig. 4. Relative effects for MCMs assembled with either KGD or WLT die.

lines represent the KGD case; solid symbols represent the WLT case. Two issues are addressed by each graph. Within a system (i.e., a KGD MCM or a WLT MCM), the slope of the line indicates the relative importance of the factor. However, in making comparisons between MCMs assembled with KGD and those assembled with WLT die, it is the difference in slope that is critical.

3.2. *Die per Module*

The number of die per module (Fig. 5) is the most critical factor for both cost and quality of an outgoing MCM, whether it is assembled with KGD or WLT die. For larger die (>0.5 cm^2) in assemblies of more than 4 die, the final MCM cost is less when KGD are used when rework is not available. For smaller die, there is a cross-over point, which is at least partially dependent on the number of die per module. In this particular analysis the cross-over point is near 10. Although the number of die becomes less critical when rework is available, it still remains one of the key factors. However, the use of rework significantly minimizes the difference between the cost of MCMs as sembled with KGD vs. WLT. In the case of the smal die after 3 rework cycles, the final MCM cost is les when WLT are used, regardless of the number of di per module.

The difference in cost between MCMs assemble with KGD vs. those assembled with WLT is essentiall eliminated with rework. However, the outgoing qual ity of the MCM assembled with KGD is always highe (Fig. 6). This is due to the lack of 100% test coverag at module test. Rework does minimize the differenc but if the die used for the repair are of lower incom ing quality (e.g., WLT vs. KGD) then the rework i also less effective. This makes the game of catch-u virtually impossible for the lower quality die.

The reason for the strong effect of number of die o module cost and quality is simply a function of proba bility which can be expressed by the equation:

$$P(zd)_{\mathrm{MCM}} = P(zd)_{\mathrm{die}}^{(\text{die per MCM})} \qquad (6$$

$P(zd)_{\mathrm{MCM}}$ Probability that there are no defects on an MCM after assembly

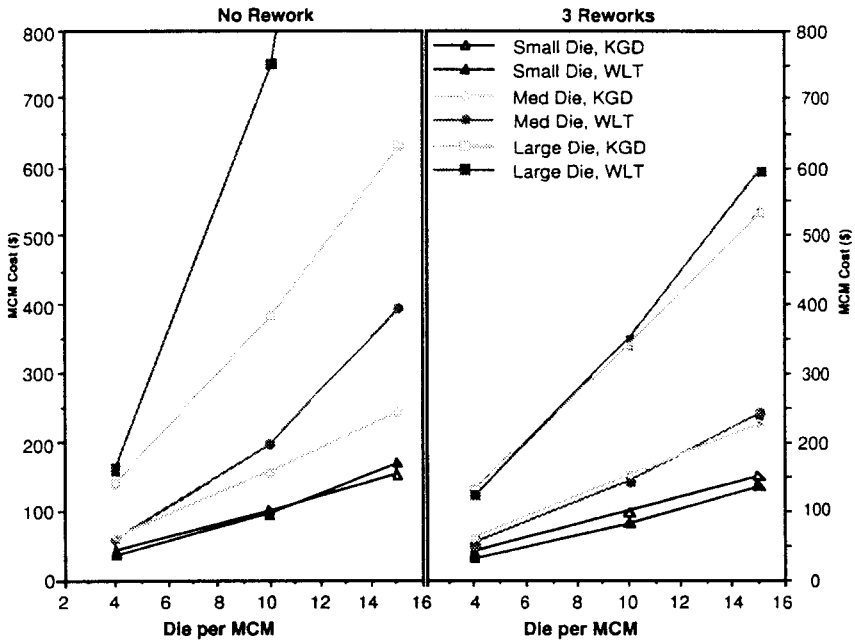

Fig. 5. Die per module vs. MCM cost.

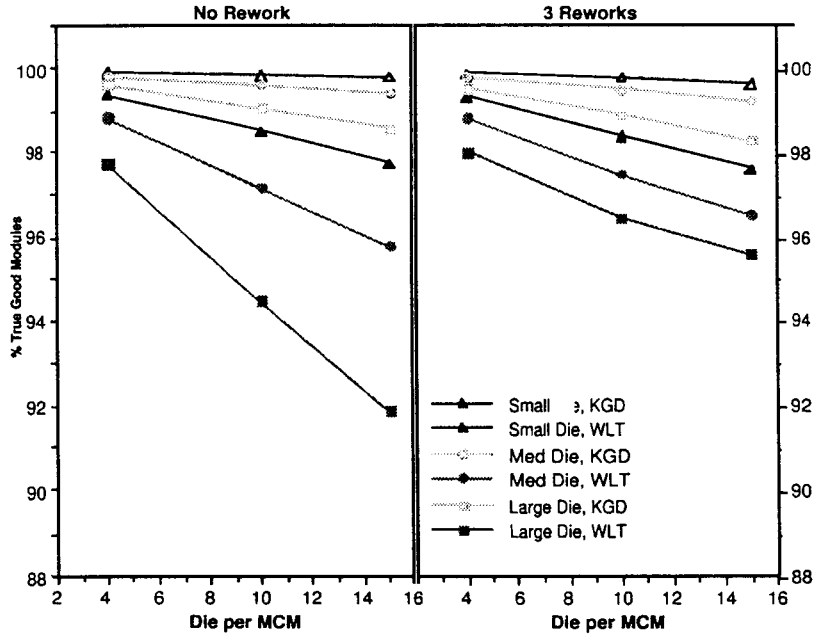

Fig. 6. Die per module vs. outgoing MCM quality.

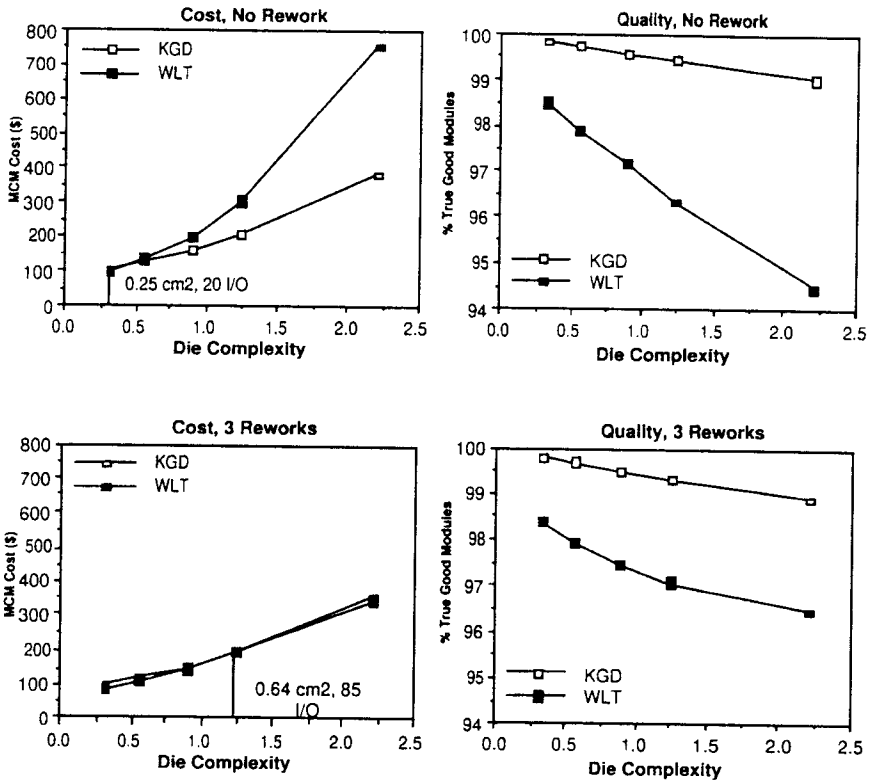

Fig. 7. Die complexity (size and pin count) vs. MCM cost and quality.

$P(zd)_{\text{die}}$ Probability that there are no defects on any given die used to assemble the MCM

It can be seen that due to the exponential nature of the relationship, the probability of a good MCM decreases rapidly as the number of die increases. As the probability of having a good module decreases, the amount of scrap increases along with the effective cost. With rework, the amount of scrap is significantly reduced and the cost of the MCM begins to approximate that of a module built with higher quality die (Fig. 5).

3.3. *Die Complexity (Size and Number of I/O)*

Die size and number of I/O have a significant impact on the cost and quality of an MCM, especially as the number of die per module increases and in the case where there is no rework. This is true for MCMs assembled with either KGD or WLT die. For the purpose of these analyses, die size and I/O count are combined into a single factor referred to as die complexity. This term is described in conjunction with Table 2 and given by Eq. (5).

As die area increases the cost of the die goes up and the yield goes down. As the number of I/O increases, the cost of assembly increases and the total yield decreases. In combination, the two factors result in more costly assemblies and increased scrap (Fig. 7). The ability to do cost-effective rework greatly impacts this effect. If the die can be adequately tested and replaced at assembly, then the cost of replacing the die roughly equals the cost of making it known good. This is seen in Fig. 7 where, after 3 rework cycles, the cost of MCMs assembled with KGD die is very nearly equivalent to those assembled with WLT die.

MCM quality is significantly affected by the use of WLT die rather than KGD when larger, higher pin count die are used (Fig. 7). Although there is some improvement after 3 rework cycles, the difference is still striking.

3.4. *Wafer-Level Test Coverage*

Test coverage at wafer-level test has a large impact on the cost of KGD modules relative to WLT modules, largely because of the effect on the latter (Fig. 8).

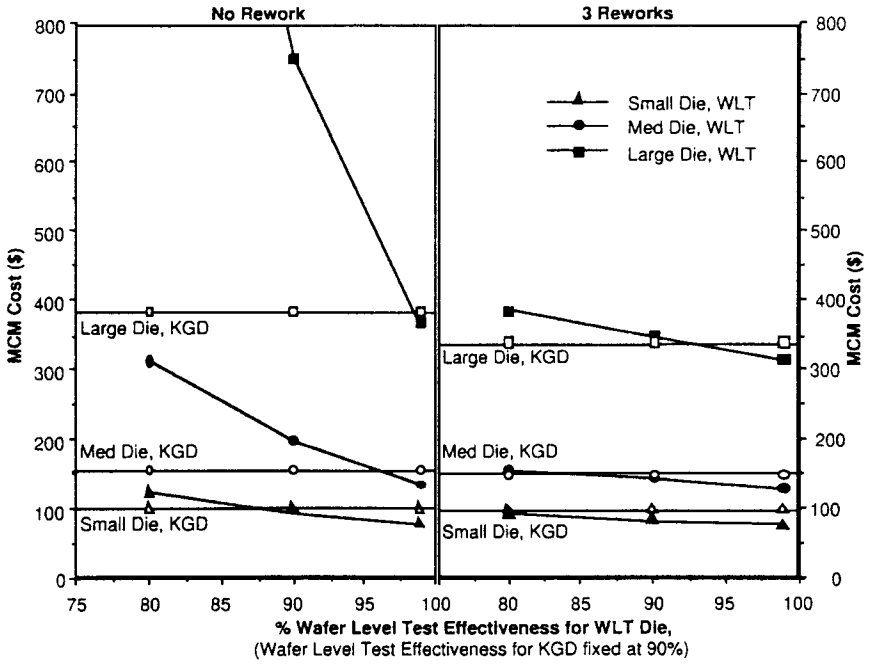

Fig. 8. Test coverage at wafer level vs. MCM cost.

Wafer-level test coverage has very little effect on the final quality or cost of modules using KGD, primarily because the test coverage at die-level test is assumed to be relatively high (minimum value of 98%, vs. 80% at wafer test). Die yields are also reasonably high since these analyses did not include very large die.

The effect of wafer-level test coverage on the cost of WLT MCMs is enhanced by an increase in die complexity; this effect is seen even after 3 rework cycles (Fig. 8). For the particular case presented, modules with small WLT die appear to be cost-effective for all levels of test coverage, with or without rework. After 3 rework cycles, even the MCMs using large die appear to be cost-effective over much of the wafer-level test coverage range. However, as can be seen in Fig. 9, the quality of the modules drops off rapidly as test coverage at wafer test is decreased below 99%.

3.5. *KGD Cost (Die-Level Burn-in and Test)*

The cost of producing KGD through die-level burn-in and test has been analyzed in a DARPA/MCC project and has been reported on in the Phase 1 final report and elsewhere [5, 7]. The results of this cost analysis indicated that as long as the reusable carrier could be utilized more than 50 to 100 times, the most significant cost drivers in controlling KGD costs are burn-in cycle time and product life. These factors were used in the present analysis to represent low and high KGD costs.

Figure 10 illustrates the relationship between the cost of performing die-level burn-in and test and the final module cost. Die complexity is also included as a factor. If rework is not an option, use of KGD makes economic sense for all but the smallest die, regardless of the cost (over the presumed range). If rework is available, then KGD costs must be held to less than the current median cost. Since this is an extremely immature technology, it is expected that costs will be continually decreasing from current values, resulting in this factor having a much smaller impact.

3.6. *MCM Rework*

Rework has been shown in the sensitivity analyses above to have a significant impact on the relative effect of most factors. Although the figures show the difference between no rework and three reworks, the biggest change occurs between zero and one, as can be seen in Fig. 11. Rework typically has a much bigger effect on the cost and quality of MCMs assembled with WLT die than with KGD.

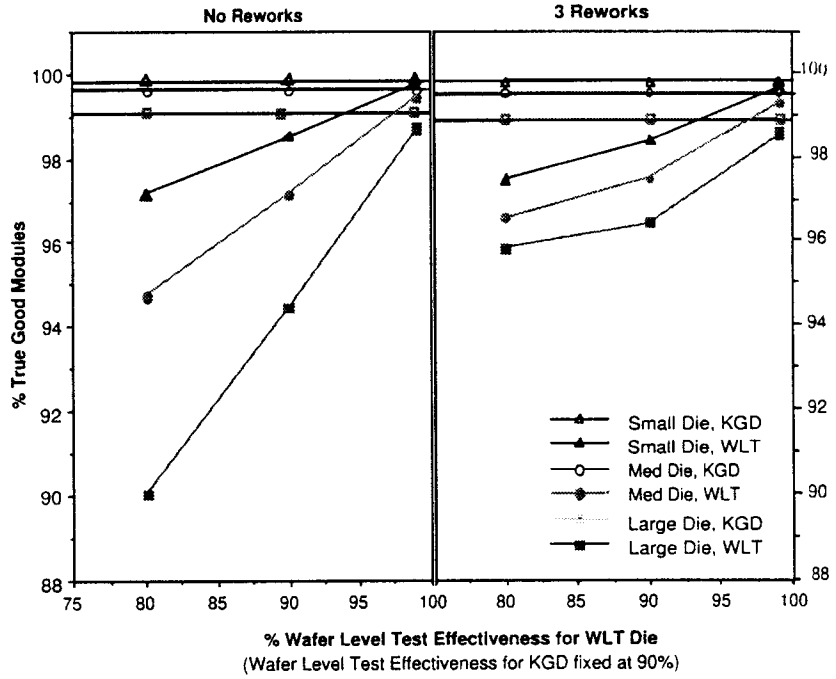

Fig. 9. Test coverage at Wafer level vs. MCM quality.

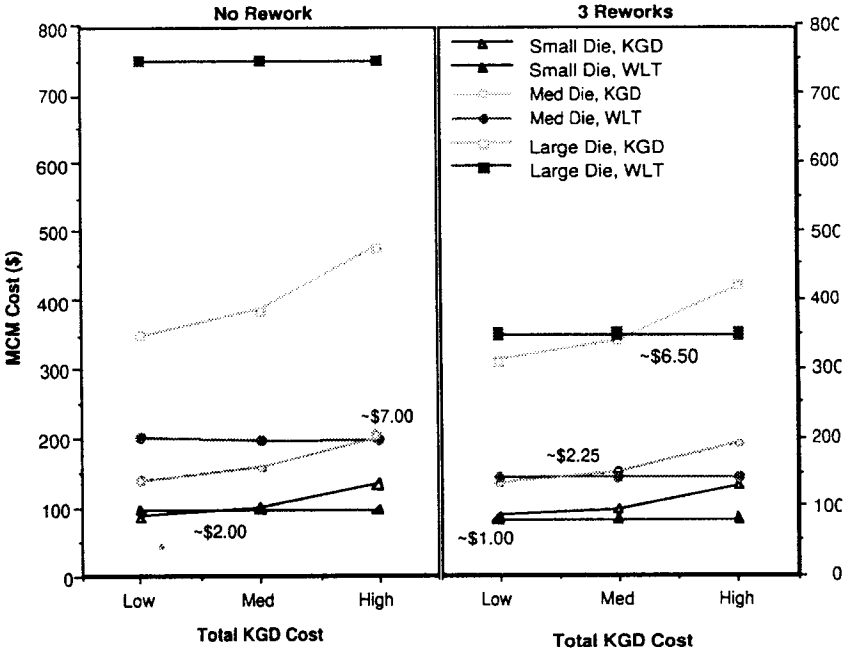

Fig. 10. Cost of producing KGD vs. MCM cost.

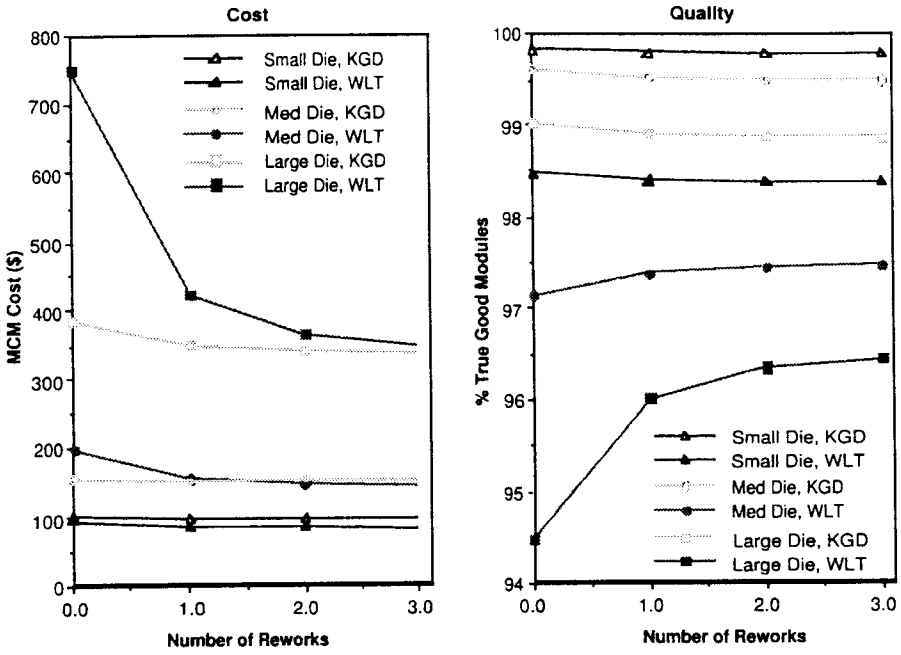

Fig. 11. Number of reworks vs. MCM cost and quality.

4. Conclusion

It has been suggested that fully tested and burned-in die are not necessary to produce cost-effective multichip assemblies, especially if one or more of the following exists:

- Rework is an option,
- The number of die per assembly is low,
- The die are relatively inexpensive,
- The incoming die are of high quality,
- The KGD process is very expensive, and
- Wafer test is very effective (high test coverage).

The analysis presented above supports this supposition; however, some of the factors were found to have a much more significant effect than others. Also, it appears that the outgoing quality of an MCM will always be less when assembled with die that have been tested only once and typically at a lower test coverage. In addition, the latent defects will be higher on the WLT MCM because of lack of burn-in. A true measure of cost-effectiveness and tradeoff analysis must take into account the cost of shipping a faulty module.

4.1. Wafer-Level Test Coverage

Modules of roughly equal quality and significantly lower cost can be assembled with die that have been through wafer-level test only, if test coverage at wafer test equals that at final test for the die-level burn-in and test die. However, as the test coverage decreases, the quality drops off rapidly and cannot be recovered through rework. If cost of quality is assumed to be 10X, test coverage at wafer test will probably have to be at least 90% (assuming rework is available) for WLT to be considered an economically viable option. In addition, without burn-in, the chances for field failures increases.

4.2. Die Complexity and Number of Die per Module

Die complexity and number of die per module have a significant impact on the relative cost of MCMs assembled with KGD die vs. WLT die only if rework is not available. If a cost-effective rework process is available, then these two factors do not have a big impact. However, if quality is taken into account, then there is a significant difference that cannot be recovered through rework.

4.3. KGD Cost

KGD cost must be kept at a moderate to low level in order for KGD MCMs to be economically viable. This is especially true if rework is an option. Although KGD does not appear to have a large effect on the outgoing quality of an MCM, it could have a significant effect

on reliability and field failures, given that the burn-in is adequate.

References

1. K. Torku and C. Radke, "Quality Level and Fault Coverage for Multichip Modules," *20th Design Automation Conference*, 1983, pp. 201–206.
2. M. Tegethoff and T. Chen, "Defects, Fault Coverage, Yield and Cost, in Board Manufacturing," *International Test Conference*, 1994, pp. 539–547.
3. Z. Sekulic, "The MCM Dilemma," *Advanced Packaging Journal*, pp. 42–45, Summer 1992.
4. J. Hagge and R. Wagner, "High Yield Assembly of Multichip Modules Through Known Good IC's and Effective Test Strategies," *Proceedings of the IEEE*, Dec. 1992, Vol. 80, No. 12, pp. 1965–1994.
5. Larry Gilg, et al., "Infrastructure of Known Good Die," *Final Report of the DARPA Funded KGD Phase 1 Project*, Microelectronics and Computer Technology Corporation, 1993.
6. C.F. Murphy, "Known Good Die Selection Tradeoffs: A Cost Model," *Proceedings of the ISHM International Conf. on Multichip Modules*, April 94, pp. 261–265.
7. M. Abadir, A. Parikh, L. Bal, P. Sandborn, and K. Drake, "Analyzing Multichip Module Testing Strategies," *IEEE Design and Test of Computers*, pp. 40–52, Spring 1994.
8. M. Abadir, A. Parikh, L. Bal, P. Sandborn, and C. Murphy, "High Level Test Economics Advisor (Hi-TEA)," *Journal of Electronic Testing (JETTA)*, Vol. 5, pp. 195–206, 1994.
9. B.T. Murphy, "Cost-Size Optima of Monolithic Integrated Circuits," *Proc. IEEE*, Vol. 52, pp. 1527–1545, 1964.
10. T.W. Williams and N.C. Brown, "Defect Level As a Function of Fault Coverage," *IEEE Trans. on Computers*, Vol. C-30, pp. 987–988, Dec. 1981.
11. V. Agrawal, S. Seth, and P. Agrawal, "Fault Coverage Requirements in Production of Testing of LSI Circuits," *IEEE Journal of Solid-State Circuits*, pp. 57–61, Feb. 1982.

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