An Analysis of the Electronic Assembly Repair Process for Lead-Free Parts Under Combined Loading Conditions

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***Abstract* - The conversion from tin-lead to lead-free electronics has created concern amongst engineers about the reliability of electronic assemblies and the ramifications that reliability changes may have on the life-cycle cost and availability of critical systems that use lead-free electronics. In this paper the impact of lead-free solder on the repair of electronic assemblies subject to combined thermal and vibration loading is studied. The cost, repair time and availability of boards are quantified using a previously developed repair simulator for a test board developed and tested by the Joint Council on Aging Aircraft & Joint Council on Pollution Prevention (JG-PP) that includes CLCC, TSOP, and PBGA packaged parts using tin-lead and lead-free solders.**

This paper describes the process of calibrating a physics-of-failure reliability simulator using experimental HALT test results for a specific board assembly and using the calibrated model to generate failure distributions corresponding to combined thermal and vibration loading over an actual product life cycle for use in the repair simulator.

The results of the repair simulation indicate that longer dwell times appear to cause more damage than larger ΔT; under combined loading conditions, SnPb appears to be more reliable than SAC (for the board and parts considered in this study) and as a result, repair cost is lower; and the number of failures and repair times track repair costs (depending on the capacity of repair process).

Index Terms - Lead-free electronics, Repair Simulation, cost, availability

I. INTRODUCTION

The impact of transitioning from tin-lead to lead-free solder parts is affecting the electronics industry and most severely the aerospace and defense industries that produce products requiring high levels of reliability, [1]. Although excluded from requirements to use lead-free parts, most defense and aerospace manufacturers must utilize the same supply chain as commercial electronics manufacturers for parts and boards. Therefore, the conversion from tin-lead to lead-free electronics is a reality and the ramifications of the conversion need to be clearly understood so that the impact of the conversion to lead-free can be quantified in order to provide performance expectations and risk mitigation.

Lead-free solders have been evaluated under various thermal and vibration test scenarios [2-11]. Tin-silver-copper (SAC) solder alloys are one of the most viable lead-free candidates for the replacement of SnPb solder due in part to its higher melting point, making it more desirable for high temperature applications. However, experimental testing has shown that SAC solders are also less durable compared to SnPb solders under vibration loading [6].

Physics of Failure simulations using lead-free solders have also been shown to provide comparable estimates of component fatigue lives to experimental thermal cycling results [5].

Various approaches have been suggested for simulating combined thermal and vibration loading conditions. Barker *et al.* [7,8] proposed a linear supposition approach (LDSA) to consider the effect of combined loading on solder joint reliability that linearly accumulates the loads. Upadhyayula and Dasgupta [9] presented an incremental damage superposition approach (IDSA) that incrementally considers the damage on solder interconnects to track nonlinear interactions between different load types of varying frequencies. Qi *et al.* [10] presented a rapid-life prediction approach (RLPA) for solder joints that captures the interactions between different loadings by considering mean stress and temperature effects on vibration response. In order to implement the rapid-life assessment model, the experimental mean stress state history in the solder joint needed to be approximated [10]; however for this study, this experimental information was not available. The IDSA requires additional experimental information: mean stress histories, discretized strain ranges, and strain transformation [11] that was not available from the experimental data. Therefore, based on the data available in the experimental data set, this paper uses the linear damage superposition approach for combining individual thermal and vibration loads.

In a previously published paper [13], the ramifications of thermal cycling on the lead-free repair process were explored using a simulation of fielded electronic systems to and through a board-level repair facility. In this model, systems manufactured with tin-lead parts or lead-free parts that are fielded, fail and have to be repaired. The model includes the effects of a finite repair process capacity, repair prioritization, multiple possible failure mechanisms, no-fault-founds, and un-repairable units. The model was used to quantify and demonstrate the system- and enterprise- level risks posed by the conversion from tin-lead to lead-free electronics under thermal cycling conditions.

In this paper, repair process trade-off results for a Joint Council on Aging Aircraft & Joint Council on Pollution Prevention (JG-PP) designed and implemented test board subjected to combined loading (thermal and vibration) are presented. The JG-PP board was experimentally tested under HALT (Highly Accelerated Life Testing) conditions, but the repair simulator models the fielding and repair of a population of LRUs (Line Replaceable Units, i.e., electronic cards or boards that may be removed from the field for repair or replacement) over a real support life (e.g., 30 years). It does not make sense to "accelerate" the repair process to the HALT conditions, therefore, in order to perform a repair simulation for the JG-PP board, reliability distributions corresponding to actual life-cycle

conditions are needed (not distributions corresponding to HALT conditions). To perform the combined loading repair simulation, a reliability simulator had to first be calibrated using the experimental HALT results for the test board (Section II). Then the calibrated model was used to evaluate the test board under actual life-cycle loading conditions (30 years) in order to generate failure distributions for the board that can be used within the repair simulator (Section III).

II. Using Experimental Random Vibration Loading Failure Distributions to Calibrate a Physics-of-Failure Reliability Simulation

This section summarizes the methodology used to calibrate the calcePWA physics-of-failure assessment simulator using experimental random vibration loading results (HALT data) for the JG-PP test vehicle [14]. The calcePWA software [12] is used to perform simulation based failure assessment of printed wiring assemblies.[1] The calcePWA software performs simulations including thermal, vibration, and failure assessment analyses for printed wiring assemblies. Once the calcePWA simulator was calibrated to the experimental failure distributions from the HALT testing, the calibrated model was used for predicting failure distributions for a vibration loading profile that could be seen during the actual support life (e.g., a 30 year time period) for the JG-PP board.

Boeing conducted a vibration test on the JG-PP test vehicle and generated CLCC-20, TSOP-50, and PBGA-225 component experimental failure distributions [14]. The study in this paper focuses on the nine components (2 TSOPs, 2 CLCCs, and 5 PBGAs) on the JG-PP board that had significant experimental failure history during vibration testing. The first step in the calibration is finding the natural frequency of the printed wiring board within the simulator and adjusting it to agree with the experimental natural frequency of the JG-PP board. It is important to match the simulated board's natural frequency to the experimental results to prevent dramatic discrepancies between simulated fatigue lives and experimental fatigue lives [8], since altering the board's natural frequency changes the vibration behavior for the entire board and thus changes the component fatigue lives. After the natural frequencies have been calibrated, the experimental vibration loads exhibited on the board must be modeled within the simulator. Once this is accomplished, the median time to failure or 50th percentile of life (N_{50}) of each simulated component on

[1] calcePWA fatigue relations for PWAs experiencing thermal cycling are described in [5] and random vibration loads are described in [15].

the board is calibrated to its experimental counterpart using a Vibration Fatigue Correction Factor (*VFCF*)[2] within the simulator. The N_{50} life was chosen for calibration because it coincides with how loading damage is assessed in the calcePWA model (temperature and vibration damage estimations based on Engelmaier and Manson-Coffin relationships are both shown in [10]). The shape parameter (β) of the simulated Weibull failure distribution was then calibrated by varying the component-specific relative board curvature (a variable that alters the vibration damage observed by the component) and conducting Monte Carlo simulations (i.e., random sampling of inputted probability distributions to arrive at different possible outcomes) at discrete percent failures to generate data that can be assessed using life data analysis software (e.g., Weibull++®).

A. Printed Wiring Board (PWB) Natural Frequency and Step-Stress Profile

The experimental first, second, and third mode natural frequencies for the JG-PP PWB are shown in Table I and compared to those found from the calcePWA simulator.

TABLE I
PWB NATURAL FREQUENCIES

Mode (F_n)	Measured Frequencies (Hz)	calcePWA Simulator Frequencies (Hz)
First Mode	72	71.5
Second Mode	101	103.2
Third Mode	210	199

The model used, only calculates the first, second, and third mode natural frequencies. It is assumed that the approximate accuracies of these modal natural frequencies are sufficient to ensure that the PWB within the simulation is under the same vibratory conditions as the experimental vehicle. The simulated natural frequencies were adjusted to match the measured natural frequencies by introducing fixed boundary conditions and adjusting the mesh density of the simulated board. These fixed boundary conditions were evenly placed along the surface area of the board to control the board's overall stiffness and arrive at an approximate representation of the experimental board's natural frequencies.

The second step to calibrate the experimental vibration loads within a physics-of-failure simulator requires the introduction and accurate representation of experimental vibration loads into the simulation tool. The experimental

[2] The *VFCF* is a multiplier in the first order vibration fatigue model. The factor scales the stress metric for a specific part and, as a result, alters that part's calculated median time-to-failure (i.e., increasing the multiplier increases the amount of damage the component receives at each exhibited vibration load) for a given vibration load profile [12].

vibration load profile is shown in Fig. 1. A step-stress random vibration profile was used in the HALT testing to achieve multiple component failures in a suitable timeframe. The testing began with a 10 G_{RMS} profile and increased in increments of 2 G_{RMS} every hour ending with a 20 G_{RMS} profile. A 28 G_{RMS} profile was then introduced for another hour at the end of the sequence to record additional component failures. The frequency ranges covered from 20 Hz to 2000 Hz, with maximum power spectral density magnitudes of each profile exhibited over the PWB natural frequencies. To model the HALT conditions in the simulation tool, a custom PSD (Power Spectral Density) curve was created for each vibration load (represented by each curve in Fig. 1) independently and then all of the loads were introduced together as one vibration load profile.

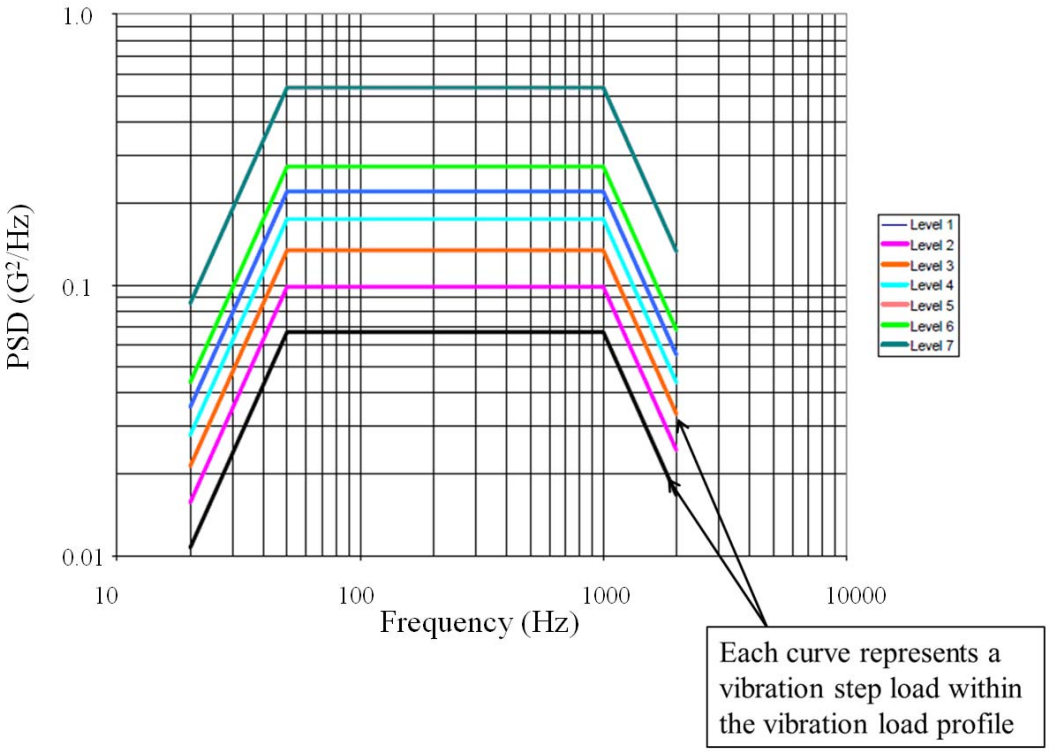


Fig. 1. Random vibration profile [14]; Level 1 corresponds to 10 G_{RMS}, Level 2 to 12 G_{RMS}, ..., Level 7 to 28 G_{RMS}.

B. Median Time to Failure (N_{50} life) Calibration

The N_{50} life is the median time to failure (50th percentile of life) of a system. The simulated N_{50} lives are calibrated within the simulator to approximate experimental median time to failures by adjusting the Vibration Fatigue Correction Factor (*VFCF*) of part/solder type combinations to match simulated results to experimental results [14]. The TSOP and CLCC parts are labeled in Fig. 2a and the *VFCF*s for each of the investigated

components are labeled at the component's location in Fig. 2b along with their corresponding solder types. In Fig. 2b, the *VFCF*s for the PBGAs appear directly on top of the corresponding component. Initially, the part/solder *VFCF*s were adjusted to fit individual component median time to failures to assess the variability of *VFCF*s among the part/solder types and locations on the board. The resulting *VFCF* variation is provided in Table II. However, the calcePWA model is not viable if every component located on the board is independently calibrated to its experimental result – the same *VFCFs* need to be applied across given part/solder types to demonstrate consistency among the types and validity of the calcePWA model. Therefore, the average *VFCF*s for a given part/solder type were found and used for each component pertaining to its particular part/solder type for the simulated failure tests, these values are given in Table II.

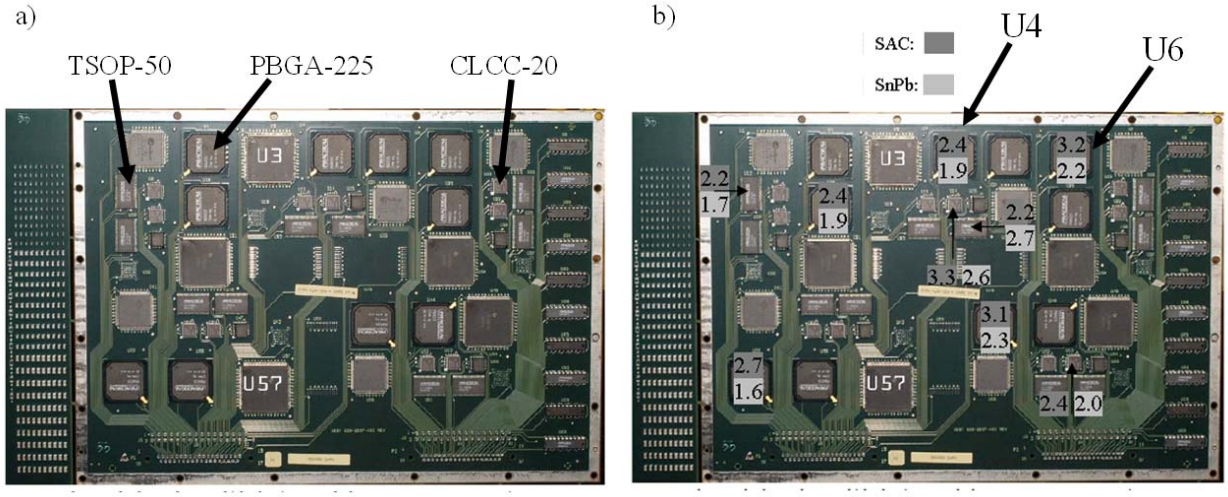


Fig. 2. JG-PP test vehicle, a) components types indicated, b) *VFCF* found for each component and location.

TABLE II
PART/SOLDER *VFCF* AVERAGES AND VARIATIONS AND VALUES USED IN SIMULATION

Part Type				VFCF Values Used	
		SAC	SnPb	SAC	SnPb
PBGA (5 components)	Average	2.76	1.98	2.8	2
	Standard Deviation	0.38	0.28		
CLCC (2 components)	Average	2.85	2.3	2.9	2.3
	Standard Deviation	0.64	0.42		
TSOP (2 components)	Average	2.2	2.2	2.2	2.2
	Standard Deviation	0	0.71		

After adjusting the *VFCF*s, the failure assessment is completed, the simulated component median TTF (time-to-failure) can be found by adding the incremental damage from each load segment. The total damage is calculated using Miner's rule (median TTF assumed when D_{total} equals 1.0) [15]:

$$D_{total} = \sum_i \frac{N_i^{applied}}{N_i^{available}} \tag{1}$$

where $N_i^{applied}$ is the number of cycles applied and $N_i^{available}$ is the number of cycles the structure can survive. Equation (1) means that the damage must be examined for each load segment and cumulatively added to obtain the component's median TTF (if the component's cumulative damage totals up to less than 1.0 through all exhibited loads, it is assumed to have survived testing). The comparison between predicted and actual median TTFs is shown in Fig. 3. The dashed and solid lines represent ± two to four lifetimes, respectively, where the one-to-one slope relationship indicates an exact correlation between experimental results and calcePWA simulated results for the nine investigated components. The ± two to four lifetime lines are used to demonstrate the validity of the calcePWA model for accurately representing experimental results using the average VFCFs found for each part/solder type component.

Fig. 3 shows the nine components that had experimental failures (not all instances of all parts failed during the experimental testing) of both the SnPb and SAC solder boards. The corresponding calcePWA simulated results for the component/solder type combinations are also shown in Fig. 3. There were five test vehicles tested with SnPb soldered components and five test vehicles with SAC soldered components. Each data point in Fig. 3 represents the experimental component median TTFs. Multiple data points of certain part/solder type combinations in Fig. 3 correspond to components at different locations on the JG-PP board. All the components experience vibration uniquely specific to their locations on the JG-PP board as shown from Fig. 2b--this explains why components of the same part/solder type may have a large variation in their median TTFs, also, the discrepancies in the component lives could be a result from individual defects within each component.

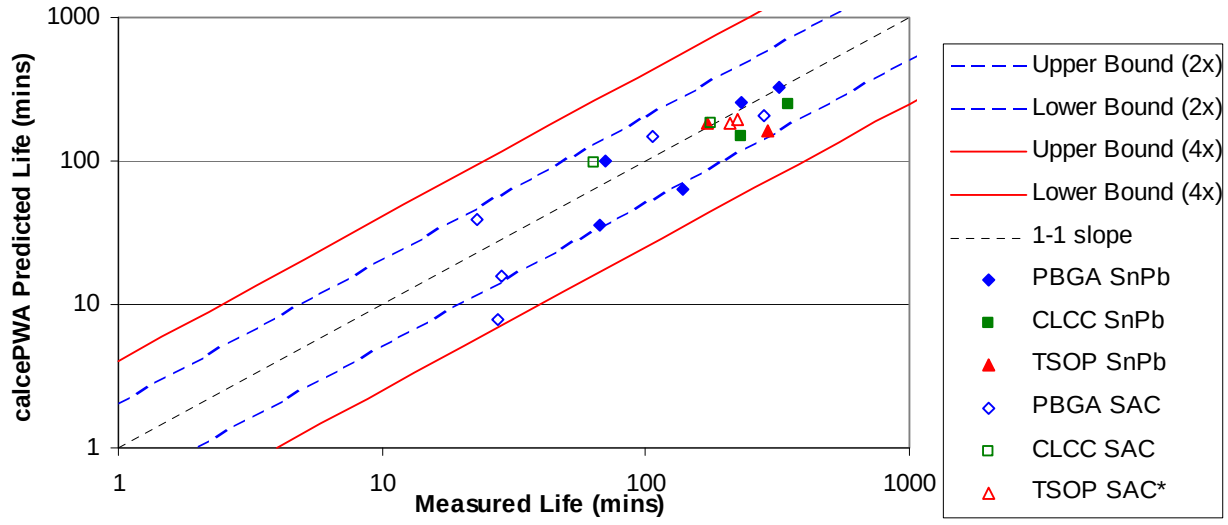


Fig. 3. Correlation of experimental N_{50} life and calibrated calcePWA simulated N_{50} life for various part types in the JG-PP subject ot HALT testing. TSOP experimental SnCu solder calibrated using calcePWA SAC solder.

Fig. 3 shows the correlation between simulated and experimental results and indicates that the calcePWA model can be calibrated to match experimental component lives to within ±4 lifetimes of the respective experimental components (PBGA, CLCC, TSOP) that were investigated. This correlation suggests that the assigned *VFCF* for each part used is sufficient for calibrating the simulated median TTF to the experimental TTF. It is also observed that the model better predicts the component life as the component life increases (i.e., there appears to be less discrepancy between predicted and measured lives). The only combination that significantly violates the ±2 lifetime boundary is one lead-free (SAC) PBGA component. In this case there was a large variation between the experimental and simulated results for this particular component on the JG-PP board. The component life variation in experimental data was large enough that calibrating the calcePWA model using a single average *VFCF* proved difficult.

Fig. 3 indicates that as the component's measured median TTF increases, the correlation between experimental and simulated component lives improves. Fig. 3 also indicates that a majority of the data points fall below the one-to-one slope regression line. This is recommended for simulation-to-experimental correlation, indicating that the simulated median TTFs occur earlier than the experimental median TTFs leading to more conservative simulated failure distributions in comparison to the experimentally analyzed failure distributions.

As the *VFCF* of a particular part increases, the component median TTF associated with that part decreases, assuming the same vibration load is applied in both cases. It is also observed that the SAC solder has a higher average *VFCF* than the SnPb solder for vibration loading. This supports prior investigations where SAC solder is deemed less reliable than SnPb solder for random vibration loading cases [6,15].

C. *Failure Distribution Calibration*

In addition to calibrating the median TTF of the failure distributions, we also wish to address the shapes of the failure distribution. Simulated failure distributions were created by applying triangular distributions to each individual component's specific relative board curvature in calcePWA for the experimental vibration profile. Monte Carlo failure assessment was then used with a sample size of 5,000 and percent desired failures were chosen and recorded.

The Weibull shape parameter (β) of the failure distributions can be adjusted by altering the amount of variation of an individual components' relative board curvature (*RBC*). By running the simulation, each unchanged component's *RBC* can be recorded (value of *a* in Fig. 4). Once this is done, unique triangular distributions (Fig. 4) can be assigned to each component where *a* is the component's unchanged relative board curvature and *b* is a fraction of *a* resulting in a lower bound of $a - ab$ and an upper bound of $a + ab$. This distribution is then applied to the currently defined load profile within the simulation. Monte Carlo failure assessment is then used for the components' specific failure model and run at specific percent desired failure increments. Once the component life assessment is completed the vibration damage is accumulated until a value of 1.0 has been reached, at which point failure is assumed to occur and the TTF can be calculated for the chosen percent desired failure. It was observed that for all individual component/solder combinations tested (see Fig. 5), when the board curvature variability used in the Monte Carlo analysis increases: the Weibull shape parameter, β, decreases and the scale parameter, η, increase.

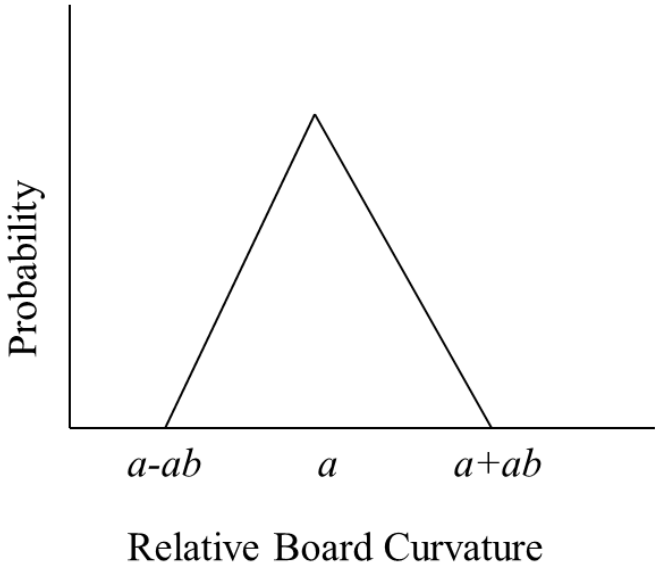


Fig. 4. Triangular parameter distribution

It is important to realize that for vibration loading, every location on the board undergoes unique vibration damage. Therefore, every experimental component had individual failure distributions that were unique to its location, part type, and solder type. This means that every component must be investigated individually to properly understand its fatigue life and behavior in relationship to the PWB.

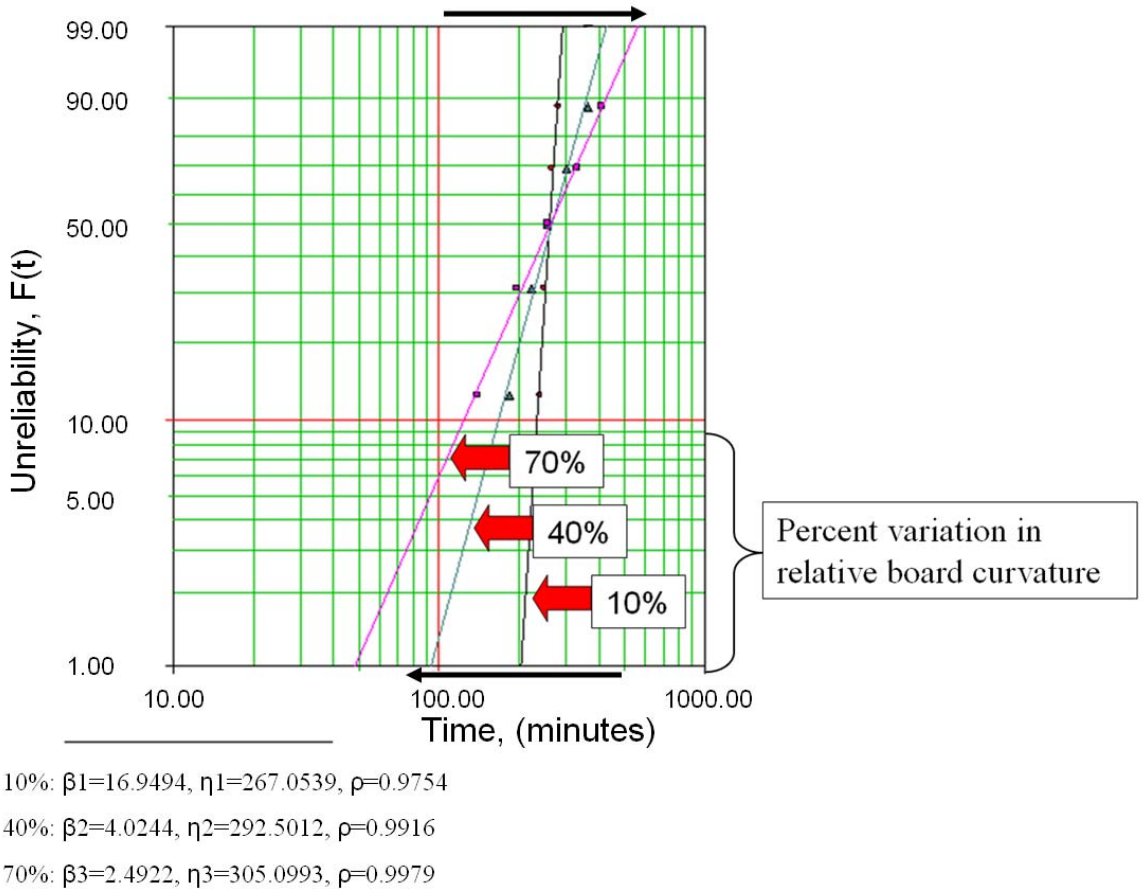
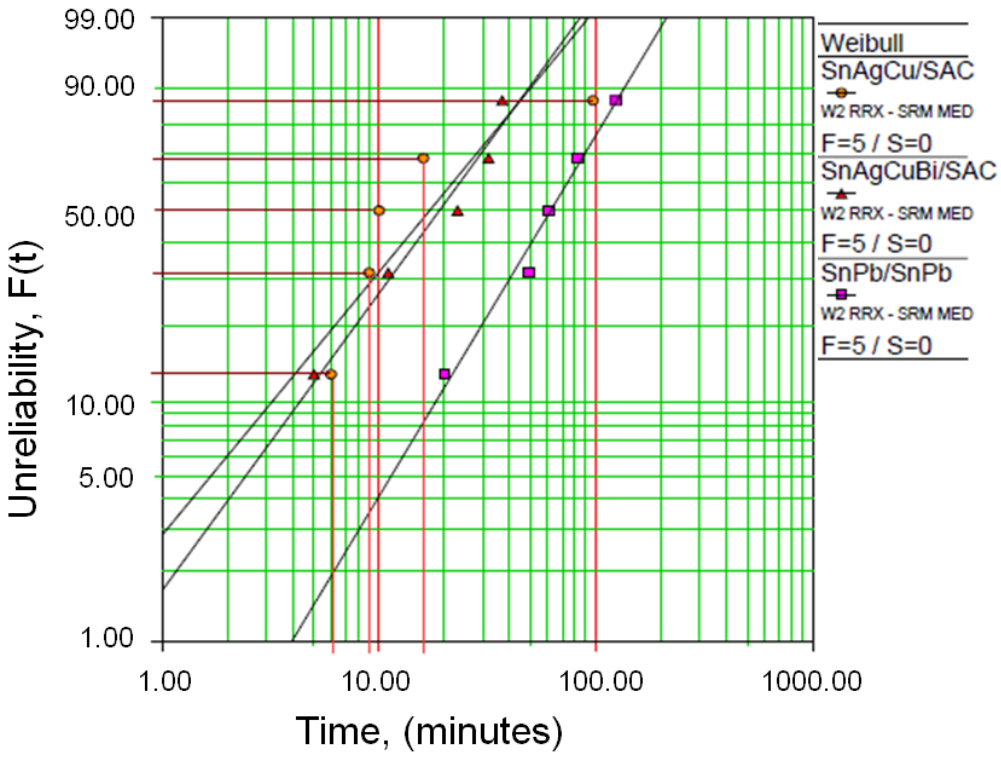


Fig. 5. Altering component *RBC* percent variation for Monte Carlo analysis results in β and η shifts in component simulated failure distributions (ρ is the correlation coefficient).

The experimental TTF data for the 18 combinations (nine components of both solder types) under investigation were analyzed using life data analysis software (Weibull++®). The TTF data was plotted at predetermined failure percentages as shown by the five horizontal lines in Fig. 6. Each component/solder combination was tested on five independent experimental test vehicles and the component TTF results were obtained. The minimum and maximum TTF data points for the experimental data are, in Fig. 6, plotted at approximately 12.5% and 88% failures, respectively (the lowest and highest of the five horizontal lines in Fig. 6). In the case where five experimental data points couldn't be obtained (i.e., there were instances where not enough experimental failures occurred), the maximum and minimum TTF data points were still plotted at 12.5% and 88% failures.



β1=1.1215, η1=23.7082, ρ=0.8501

β2=1.2672, η2=25.3196, ρ=0.9831

β3=1.5387, η3=78.5989, ρ=0.9901

Fig. 6. Experimental Weibull for PBGA U4 (five recorded failures for SAC & SnPb) subject to HALT testing (ρ is the correlation coefficient).

A calibration similar to the experimental analysis and data representation described above in Fig. 6 was then conducted for the calcePWA model. The ranges (measured time between the earliest recorded failure and latest recorded failure) of the experimental TTF data were recorded for each individual component/solder type combination and used for calibration purposes through varying the relative board curvature for individual components of part/solder types. This comparison is shown through horizontal error bars (range of measured life data) and vertical error bars (range of calcePWA predicted life data) for the investigated components and can be seen in Fig. 7.

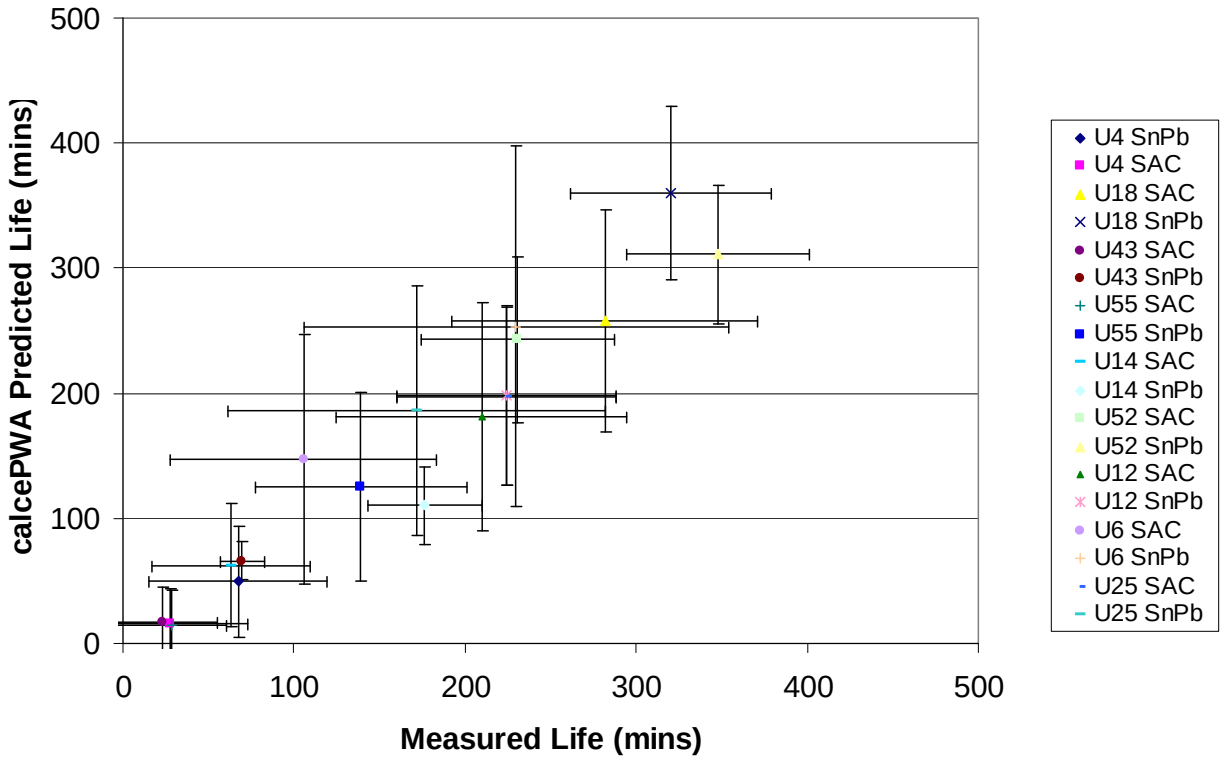


Fig. 7. Experimental TTF range (horizontal-error bars) versus predicted TTF range (vertical-error bars) subject to HALT testing.

Fig. 7 represents the time to failure range difference between the experimental components and their simulated counterparts by varying the relative board curvature used in conducting Monte Carlo failure assessment. All experimental ranges versus simulated ranges were less than 50% different from one another, leading to the assumption that accurately relating experimental and predicted TTF ranges lead to successful shape calibration of the failure distribution. The final TTF distributions (simulated compared to experimental) for the U6 (PBGA) component are shown in Fig. 8.

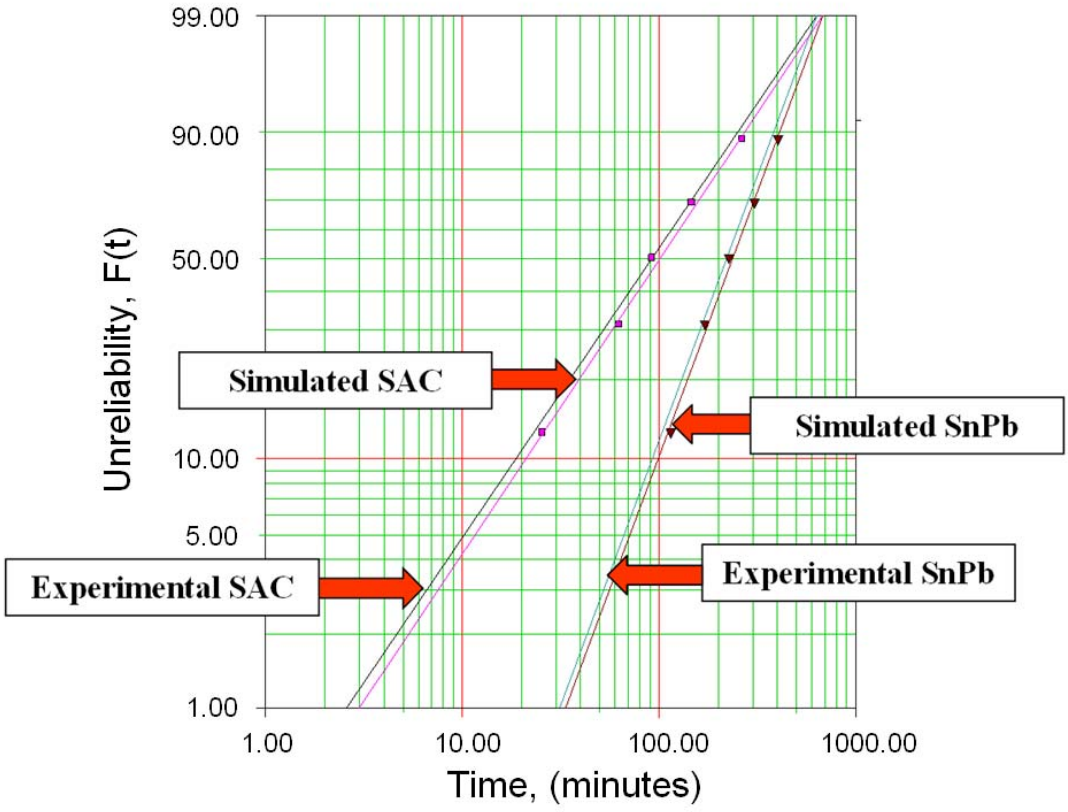


Fig. 8. Component U6 (PBGA) median time to failure and β calibration subject to HALT testing (ρ is the correlation coefficient, note ρ has a value of 0 for the experimental data because no fit is included).

D. Predicting Failure Distributions

At this point the simulator has been calibrated to HALT experimental vibration results, the next step is to implement the component-specific conditions (*VFCF* and relative board curvature variation) obtained from calibration for a different vibration load profile to predict failure distributions that can be used in the repair simulator.

A thirty-year profile for jet aircraft vibration exposure shown in Fig. 9. The profile shown in Fig. 9 was used in calcePWA and simulated failure distributions for the thirty-year load profile were obtained using the component-HALT calibrated conditions for the previous case. An example of predicted failure distributions using the

component-HALT calibrated conditions is shown in Fig. 10. Fig. 10 shows two of the 18 predicted failure distributions generated (nine components for both solder types tested).

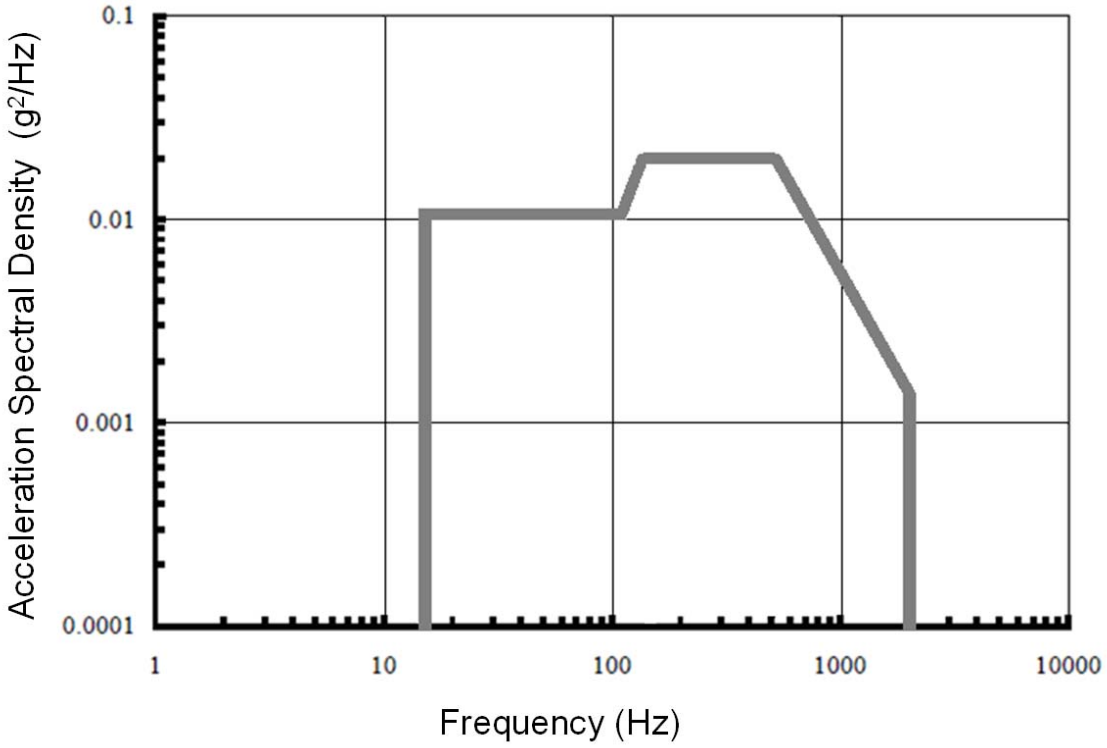


Fig. 9. General Random Vibration Exposure Profile [17].

The most conservative (judged from component median TTF and Weibull slope) component TTF distribution is used for each part/solder combination for implementation into the repair simulation in order to simulate worst-case scenarios.

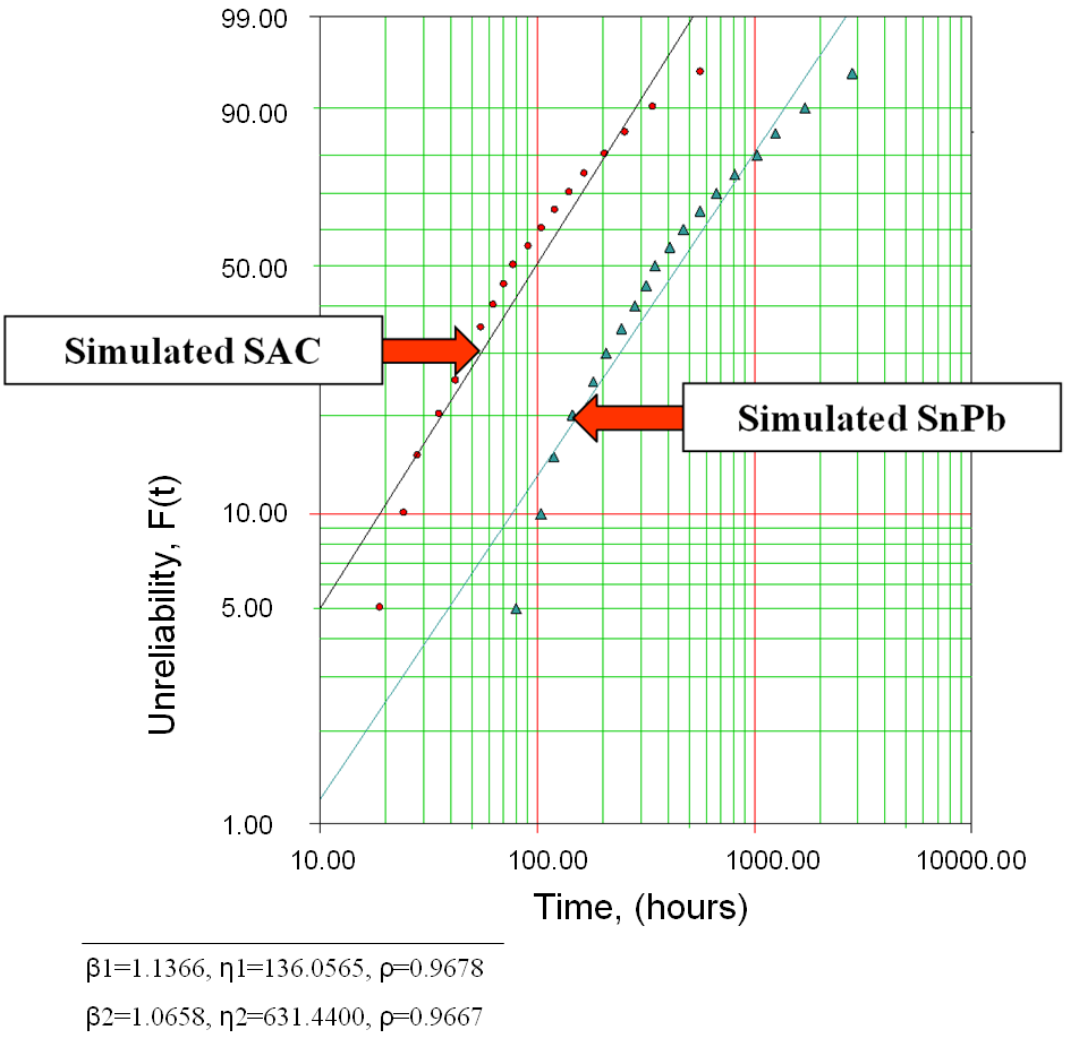


Fig. 10. Component U4 (PBGA) predicted failure distribution based on component-HALT calibrated conditions (ρ is the correlation coefficient).

III. Combined Loading (Thermal and Vibration) Impacts on Lead-Free Electronic Assembly Repair

This section summarizes the trade-off results from the Lead-Free Dynamic Repair Simulator (LFDS) [13] for the JG-PP board subject to combined loading (thermal and vibration).

The process of calibrating calcePWA for vibration loading was described in Section II. After calcePWA was calibrated, real support life load profiles (e.g., 30 years) were introduced and new failure distributions were generated using component-HALT calibrated conditions. These failure distributions were then implemented within LFDS and trade-off results were recorded. Three combined loading cases were investigated, each with varying thermal cycling loads and cycle times [13]. These three cases and their information are described in Table III. The

three cases were investigated in order to determine any relationship between both solder types and how varying thermal load profiles affects total repair costs, repair time per LRU, and availability. The dwell time characterizes the duration of time spent at the maximum and minimum temperatures of a given temperature cycling profile.

TABLE III
THERMAL CYCLING CASES IN COMPARING SOLDER RELIABILITY

Case #	Maximum Temp (°C)	Minimum Temp (°C)	Mean Temp (°C)	Dwell Time (min)
1	130	0	65	0.1
2	110	0	55	10
3	100	0	50	40

A. Combined Thermal and Vibration Loading Simulator Calibration

The thermal cycling calibration using calcePWA based on experimental thermal cycling results for the JG-PP board [18] was performed by adjusting the Thermal Fatigue Calibration Factor (*TFCF*).[3] The thermal loading and vibration loading cases are run independently within calcePWA. The repair simulator assumes independence of the two life-cycle loads, i.e., linear damage superposition is assumed.

After the thermal and vibrational life cycle loads were found separately within calcePWA, the loads were then combined using the Linear Damage Superposition Approach (LDSA). This formula assumes independence between the interactions of both loads, [8]:

$$D_{total} = D_v + D_{th} = n_{th}\left(\frac{f_v \big/ f_{th}}{N_v} + \frac{1}{N_{th}}\right) \tag{2}$$

$$N_f = \frac{1}{D_{total}} \tag{3}$$

in (2), the subscripts "*th*" are for thermal and "*v*" for vibration, and

D = damage
n = cycles experienced
f = frequency of loading
N_f = solder joint fatigue life

[2] The *TFCF* is a multiplier on the first order thermal fatigue model. The factor scales the stress metric for a specific part and, as a result, alters that part's calculated median time-to-failure for a given thermal load profile [12].

After the two load profiles (thermal and vibration) cases were combined using LDSA (both loads were accumulated using a common timescale and then converted to cycles based upon the cycle time for each respective thermal case), the final combined failure distributions were calculated within Weibull++ and are given in Table IV.

TABLE IV
CALCEPWA PART/SOLDER SPECIFIC FAILURE DISTRIBUTIONS

	Solder Type	SnPb		SAC	
	Weibull Parameter	β	η (cycles)	β	η (cycles)
PBGA	Case 1: 0-130 °C 0.1 min dwell	1.5483	1508.1182	1.169	589.6237
	Case 2: 0-110 °C 10 min dwell	1.2309	958.9214	1.15	257.7426
	Case 3: 0-100 °C 40 min dwell	1.1146	390.6787	1.139	90.2103
CLCC	Weibull Parameter	β	η (cycles)	β	η (cycles)
	Case 1: 0-130 °C 0.1 min dwell	4.7439	804.1799	1.847	847.8264
	Case 2: 0-110 °C 10 min dwell	3.7462	944.0726	1.4959	546.6333
	Case 3: 0-100 °C 40 min dwell	2.8534	677.253	1.255	257.4231
TSOP	Weibull Parameter	β	η (cycles)	β	η (cycles)
	Case 1: 0-130 °C 0.1 min dwell	2.3197	1324.1623	1.7174	2038.635
	Case 2: 0-110 °C 10 min dwell	1.9149	2062.17	1.4625	2101.653
	Case 3: 0-100 °C 40 min dwell	1.5635	2609.2684	1.2185	1931.075

B. Repair Simulator Inputs

The LFDS repair simulator is described in detail in [13]. All of the non-part and board-specific inputs for the case study described in this section are identical to the inputs described in [13] and will not be repeated here. Briefly, LRUs are introduced quarterly over a ten-year period with a smooth introduction rate and an equivalent retirement rate during a ten year period. Each LRU has a support life of exactly 30 years over which it will experience 1000 operational cycles. A repair process that follows the NSWC Crane aviation repair process consisting of 48 independent process steps is assumed – see [13] for a detailed description of this process. In this case study a population of 8,000 LRUs is modeled. Each LRU has the assigned part failure distributions for a given

case/solder type to determine the repair cost per LRU, availability, and repair time per LRU – see [13] for a description of how these output metrics are measured.

C. Case 1: 130 °C maximum, 0.1 min dwell

The first case is the least damaging of the three cases as it has the shortest dwell time of 0.1 minutes, 99%. The total repair cost, availability, and total repair times per LRU can be seen in following Figs. 11-13.

The repair cost per LRU distribution shows that, on average, the lead-free soldered LRU costs $8,629 where the SnPb soldered LRU average cost is $4,122. The availability distribution shows that lead-free soldered LRUs were available, on average, 99.7% of the time while SnPb soldered LRUs were available, on average, 99.8% of the time. For case 1, the SnPb solder is more reliable and less expensive than SAC solder.

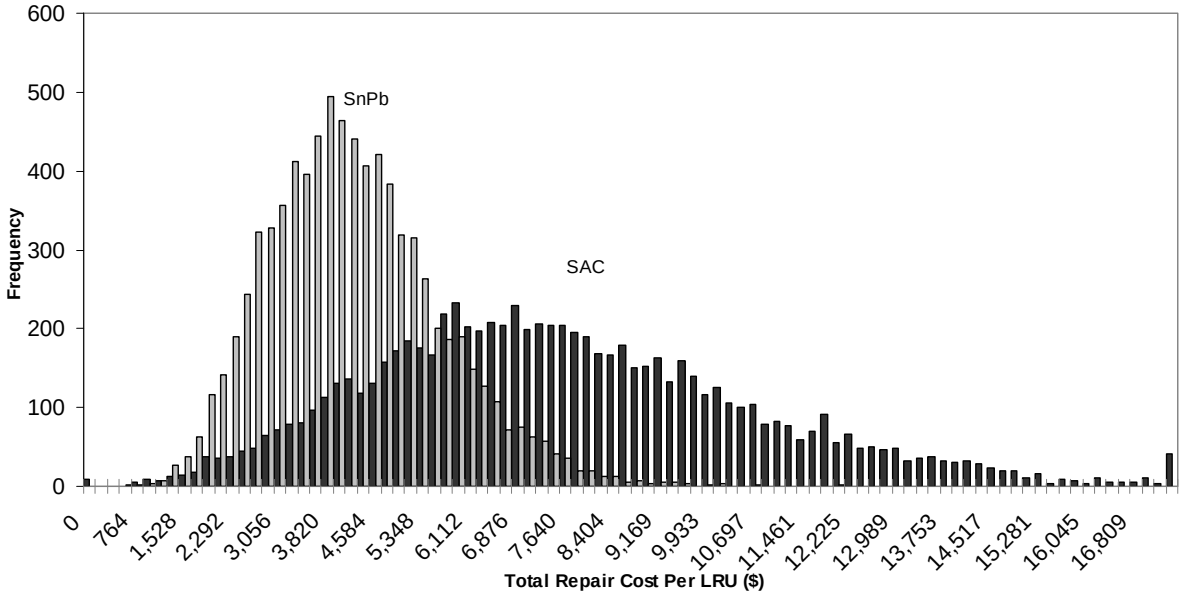


Fig. 11. Case 1 comparison of repair cost per LRU for SnPb and SAC.

Fig. 13 shows the total repair time per LRU for both solder types. The average repair time for lead-free soldered LRUs is 25 days; the average repair time for SnPb is 17 days. For case 1, the SnPb solder is more reliable and on average, half as expensive, as SAC solder.

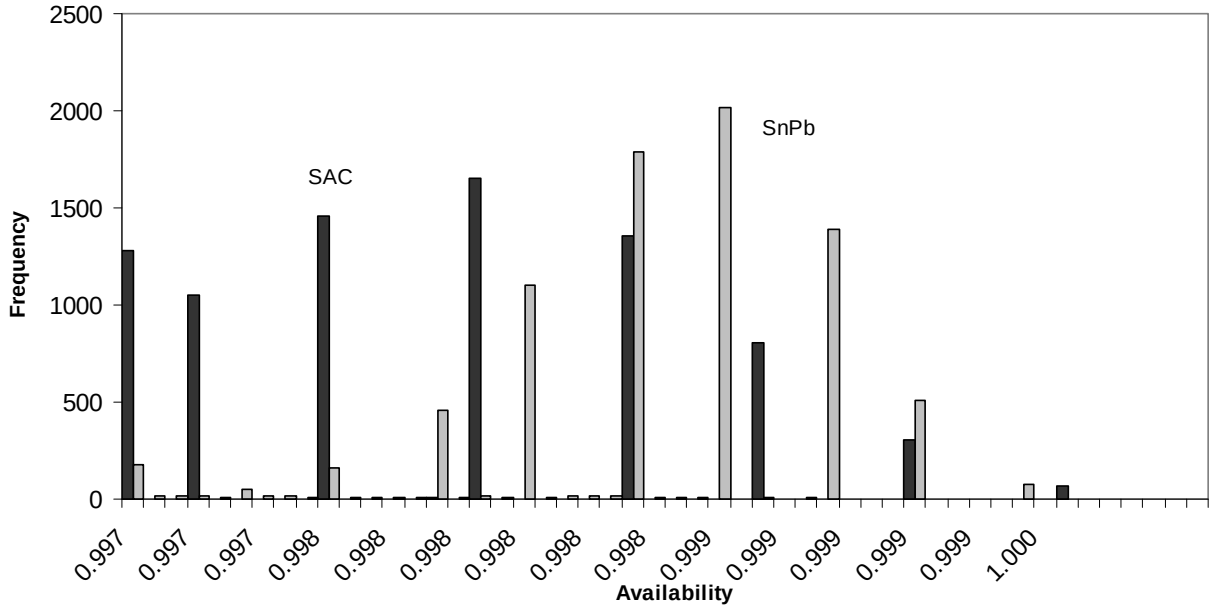


Fig. 12. Case 1 comparison of availability per LRU for SnPb and SAC.

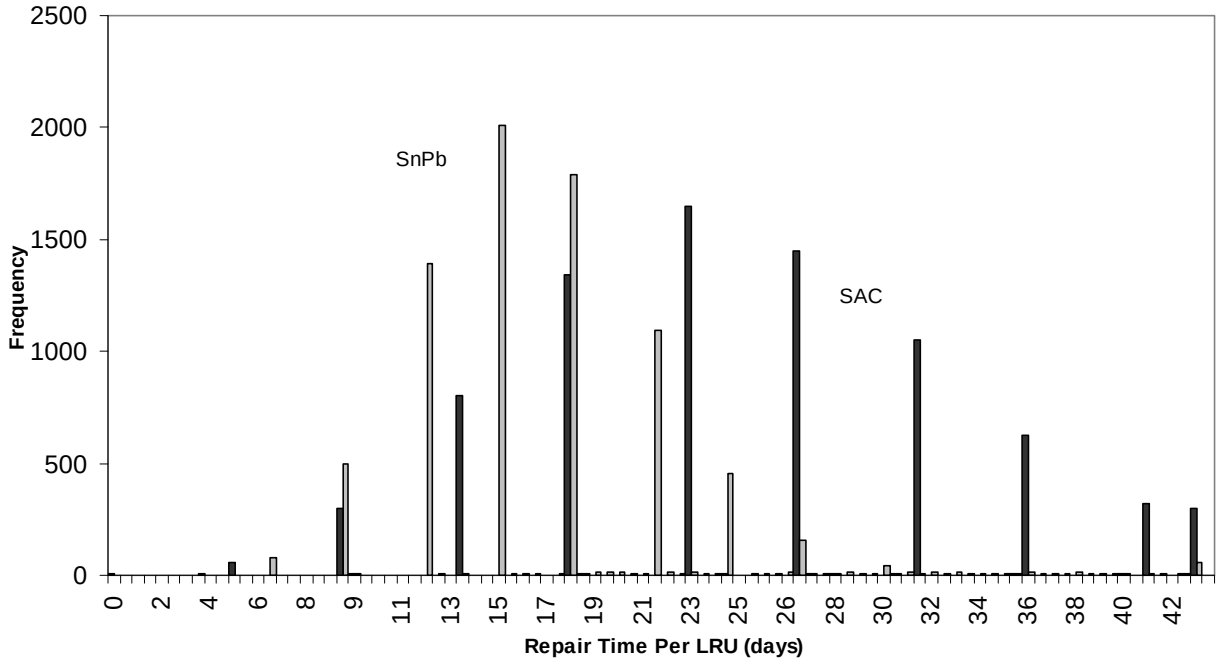


Fig. 13. Case 1 comparison of repair time per LRU for SnPb and SAC.

D. Case 2: 110 °C maximum, 10 min dwell

The second case involved a 99% increase in the dwell time of the thermal cycling profile over case 1. The result of the increase in the dwell time is an increase in the life-cycle cost for both types of soldered LRUs. The total repair cost, availability, and total repair times per LRU can be seen in following Figs. 14-16.

The repair cost per LRU distribution shows that, on average, the lead-free soldered LRU costs $15,492 where the SnPb soldered LRU average cost is $4,621. The introduction of a longer dwell time and smaller ΔT thermal cyclic load results in an increase in the number of SnPb soldered LRUs that never fail and therefore have no repair cost and an availability of 1.0. The availability distribution shows that lead-free soldered LRUs were available, on average, 99.5% of the time while SnPb soldered LRUs were available, on average, 99.8% of the time. For case 2, the SnPb solder is more reliable and less expensive than SAC solder.

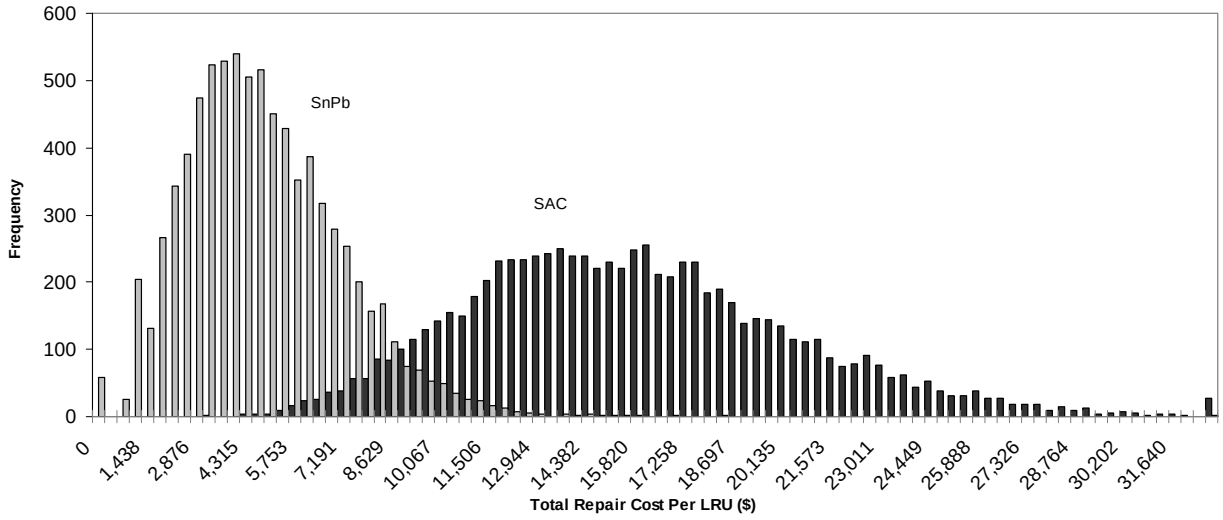


Fig. 14. Case 2 comparison of repair cost per LRU for SnPb and SAC.

Fig. 16 shows the total repair time per LRU for both solder types. The average repair time for lead-free soldered LRUs is 48 days; the average repair time for SnPb is 17 days. For case 2, the SnPb solder is more reliable and on average 3.35 times less expensive than SAC solder.

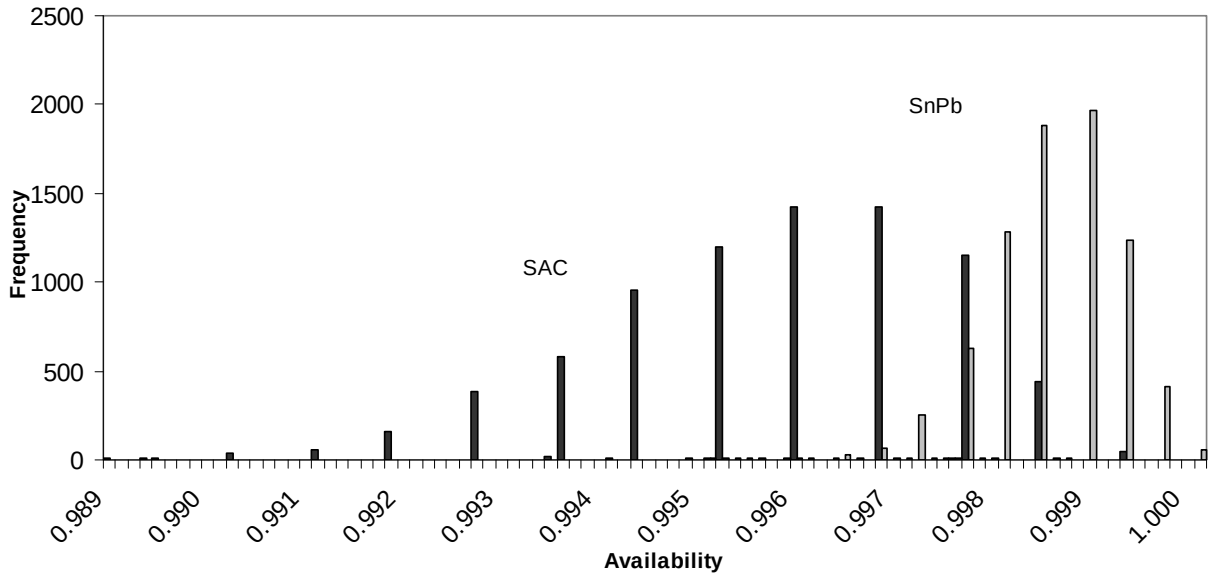


Fig. 15. Case 2 comparison of availability per LRU for SnPb and SAC.

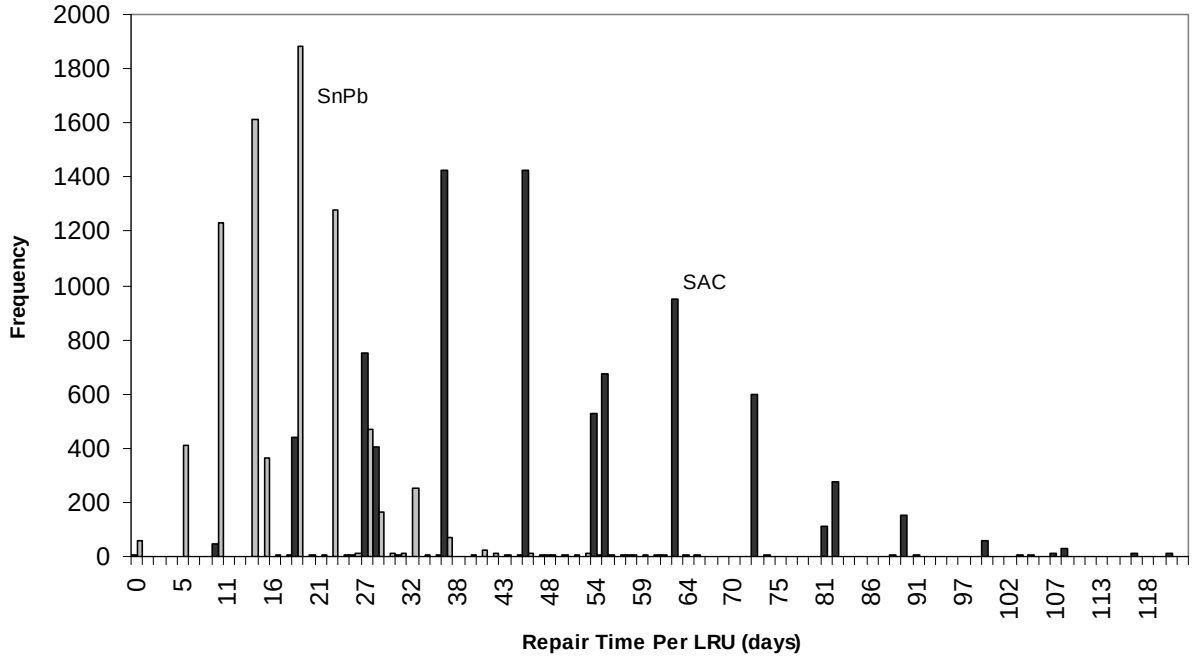


Fig. 16. Case 2 comparison of repair time per LRU for SnPb and SAC.

E. Case 3: 100 °C maximum, 40 min dwell

The third case under investigation involves the longest dwell time of the three cases. Although the maximum temperature is lower than cases 1 and 2, the longer dwell time causes the most damage out of the three cases

investigated. The maximum and minimum temperatures would have more of an effect on the component TTF distributions if the variation was larger (i.e., if the minimum went below 0°C); however, of the cases under consideration the dwell time is the major driver that shortens the component TTFs for both SnPb and SAC solders. The total repair cost, availability, and total repair times per LRU can be seen in following Figs. 17-19.

The repair cost per LRU distribution shows that, on average, the lead-free soldered LRU costs $37,453 where the SnPb soldered LRU average cost is $10,466. The availability distribution shows that lead-free soldered LRUs were available, on average, 98.9% of the time while SnPb soldered LRUs were available, on average, 99.6% of the time. There are instances observed with SnPb soldered LRUs for this case characterized as having no repair cost and an availability of 1.0. These instances indicate that the LRU in question never failed during its field life and therefore was always available.

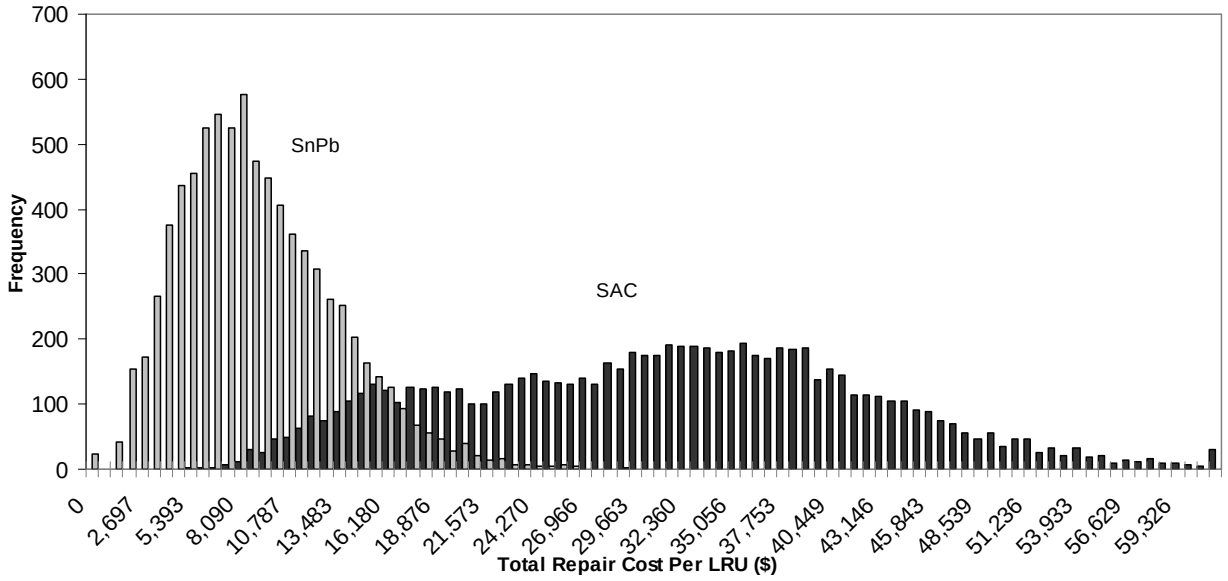


Fig. 17. Case 3 comparison of repair cost per LRU for SnPb and SAC.

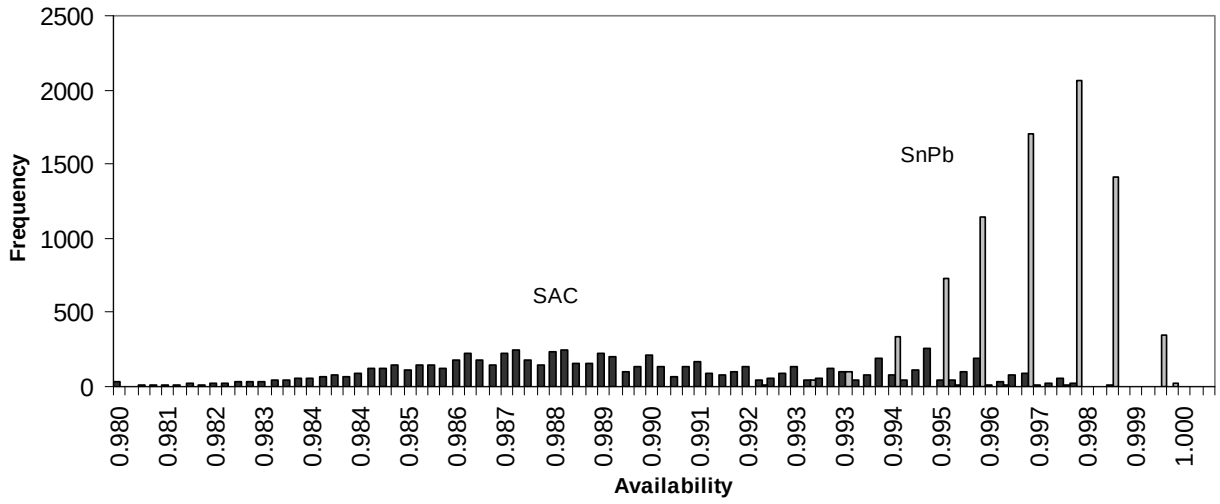


Fig. 18. Case 3 comparison of availability per LRU for SnPb and SAC.

Fig. 19 shows the total repair time per LRU for both solder types. The average repair time for lead-free soldered LRUs is 118 days; the average repair time for SnPb is 34 days. For case 3, the SnPb solder is more reliable and on average 3½ times less expensive than SAC solder.

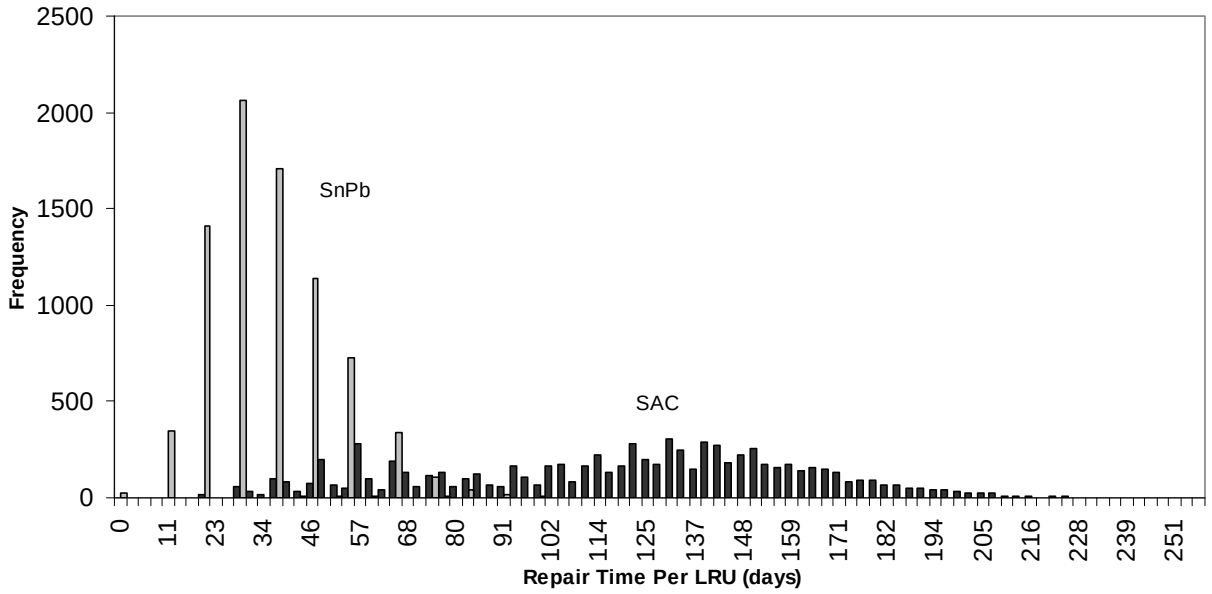


Fig. 19. Case 3 comparison of repair time per LRU for SnPb and SAC.

IV. Discussion and Conclusions

The summary of the three cases for solder reliability considered in this study is shown in Table V. For the combined loading cases, it is seen that the SnPb solder were on average less expensive and more reliable compared to the SAC solder for each investigated case. This is explained in part due to the vibration load that comprises the majority of the damage accumulated from the combined loading profiles. In vibration testing, it was observed that SnPb was more reliable than SAC [6,16], so it is understandable why these results are similar for the combined loading cases.

TABLE V
SOLDER RAMIFICATIONS FOR COMBINED LOADING (% DIFFERENCES BETWEEN SnPb AND SAC, POSITIVE NUMBERS INDICATE THAT SAC > SnPb)

	Thermal Cycling Only			Combined Loading (with vibration)		
Case	Case 1: 0-130 °C 0.1 min dwell	Case 2: 0-110 °C 10 min dwell	Case 3: 0-100 °C 40 min dwell	Case 1: 0-130 °C 0.1 min dwell	Case 2: 0-110 °C 10 min dwell	Case 3: 0-100 °C 40 min dwell
Mean Number of Failures per LRU	290%	1.90%	-28%	50%	167%	228%
Mean Repair Cost	423%	4.40%	-32%	109%	235%	258%
Mean Availability	-0.20%	0.00%	0.08%	-0.07%	-0.28%	-0.76%
Mean Repair Time	272%	1.30%	-27%	48%	178%	243%

Table V summarizes the repair ramifications in the movement from tin-lead to lead-free solder in electronic assemblies concerning thermal cyclic loading [13] and combined loading (thermal and vibration). It was observed that for thermal cyclic loading only, SAC solders are more reliable and lead to lower life-cycle costs compared to SnPb solders concerning thermal cycles with long dwell times. As the dwell time increases and the ΔT decreases, SAC soldered components have a higher reliability and lower life-cycle cost compared to SnPb soldered components.

In the case of combined thermal and vibration loading, SAC soldered components are observed to be less reliable and have higher life-cycle costs compared to SnPb soldered components for all test cases considered. However, as the dwell time decreases and the ΔT increases, the SAC solder reliability and life-cycle costs become more comparable to the SnPb solder counterpart. The results between the two studies (thermal cycling only and

combined loading) show opposing trends; the best explanation for this discrepancy can be attributed to the fact that investigated LRUs for both product life cycle cases did not contain the same components in addition to the varying component parameters, types, and calibration techniques used between both investigations.

There are several opportunities for future work that extend the work in this paper. The case study results indicated that random vibration caused the majority of the damage under the investigated combined loading conditions for LRUs containing CLCC, TSOP, and PBGA packaged parts. However, few studies have been conducted that compare the effects of tin-lead and lead-free solder reliability and ramifications (repair cost, availability, and repair time) under different vibration loading conditions (i.e., random vibration versus harmonic vibration). Furthermore, the analysis of the electronic assembly repair process concerning lead-free parts under combined loading conditions should be expanded to include similar investigations that involve IDSA [9,11] and RLPA [10] superposition techniques.

ACKNOWLEDGMENTS

The authors also wish to thank Bill Russell at Raytheon and Denny Fritz at SAIC for their contributions to this research, and the Naval Surface Warfare Center at Crane Indiana for providing data and technical feedback. The authors would also like to thank the more than 100 companies and organizations that support research at the Center for Advanced Life Cycle Engineering (CALCE) at the University of Maryland annually.

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