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SYSTEM-LEVEL IMPACT OF EARLY PACKAGING DECISIONS

Chet A. Palesko and Peter A. Sandborn
Savantage, Inc.
3925 W. Braker Lane, Suite 325, Austin, Texas 78759-5321
{chet, sandborn}@savantage.com

ABSTRACT

As system designers drive systems to be "cheaper, better, faster, and smaller", the impact of packaging decisions on the physical characteristics of the system is growing. A methodology called "System Virtual Prototyping" is outlined that brings analysis and optimization of these tradeoffs to the front of the system design process. The key to this methodology is combining accurate manufacturing information with design information to optimize the system characteristics. An example, which was analyzed with the SavanSys™ system virtual prototyping software, is presented. The example shows how the use of a more expensive micro-via laminate substrate technology can result in a less expensive system than conventional printed wiring board substrate technologies under application specific design conditions.

I. ELECTRONIC SYSTEM DESIGN

Electronic systems are composed of a hierarchy of chip and packaging technologies including bare die, die bonding, single chip packages, modules/boards, connectors, backplanes, and cooling structures. The key to successful electronic system design is to find the optimum combination of components and technologies in this hierarchy to meet cost and performance goals.

A. Electronic System Drivers

Designers of electronic systems are continually driven to deliver new products that are "cheaper, better, and faster". The need to simultaneously improve all three has been evident in the electronics industry for the last twenty years. For example, 200 MHz personal computers are common today compared to 133 MHz machines last year. Today's 200 MHz computers are cheaper than their slower counterparts were last year, and a typical system comes with a multi-gigabyte disk drives, a high-speed CD-ROM drive, and a 33.6Kbps modem.

In recent years, however, a new driver has been added to the "cheaper, better, faster" trio. The "Portable Office" is now also driving electronic systems to be smaller. Historically, making electronic systems smaller has not been as significant as it is today. Mainframe computers were large enough to accommodate a lot of electronics, and even workstations had ample room for circuitry. With the recent explosive growth in handheld and portable devices, more electronics must fit into smaller spaces. Portable and laptop computers are two of the fastest growing segments in the computer industry and both have extreme space challenges.

This confluence of four key electronic system drivers has put tremendous stress on the electronic packaging for systems. In particular, the three following factors drive designers to use advanced packaging and interconnect concepts such as MCMs, advanced single chip packages, and micro-via boards.

Larger silicon: More capability is being integrated into individual die. This results in larger die with more I/Os. Modern ASICs have hundreds of I/Os, and getting an I/O from the silicon to the rest of the system is not easy with traditional packaging and conventional printed wiring board technology containing only a few routing layers.

Faster Clock Rates - In order to get faster systems, system clock rates and chip clock rates have steadily grown. At system clock rates of 100 MHz and over, traditional PWBs with traditional single chip packaging have extremely difficult interconnection issues related to timing.

Higher Density Circuits - Driven by the need to make systems smaller, more electronics must fit into smaller spaces. Traditional packaging techniques and printed wiring boards were initially designed to fit into backplanes and do not work effectively for portable devices due to their relatively low density.

If it were not for the economic constraint (cheaper), the choice would be easy. MCMs and other types of advanced packaging and board technology would be used extensively for all leading edge electronic system designs challenged with "faster, smaller, and

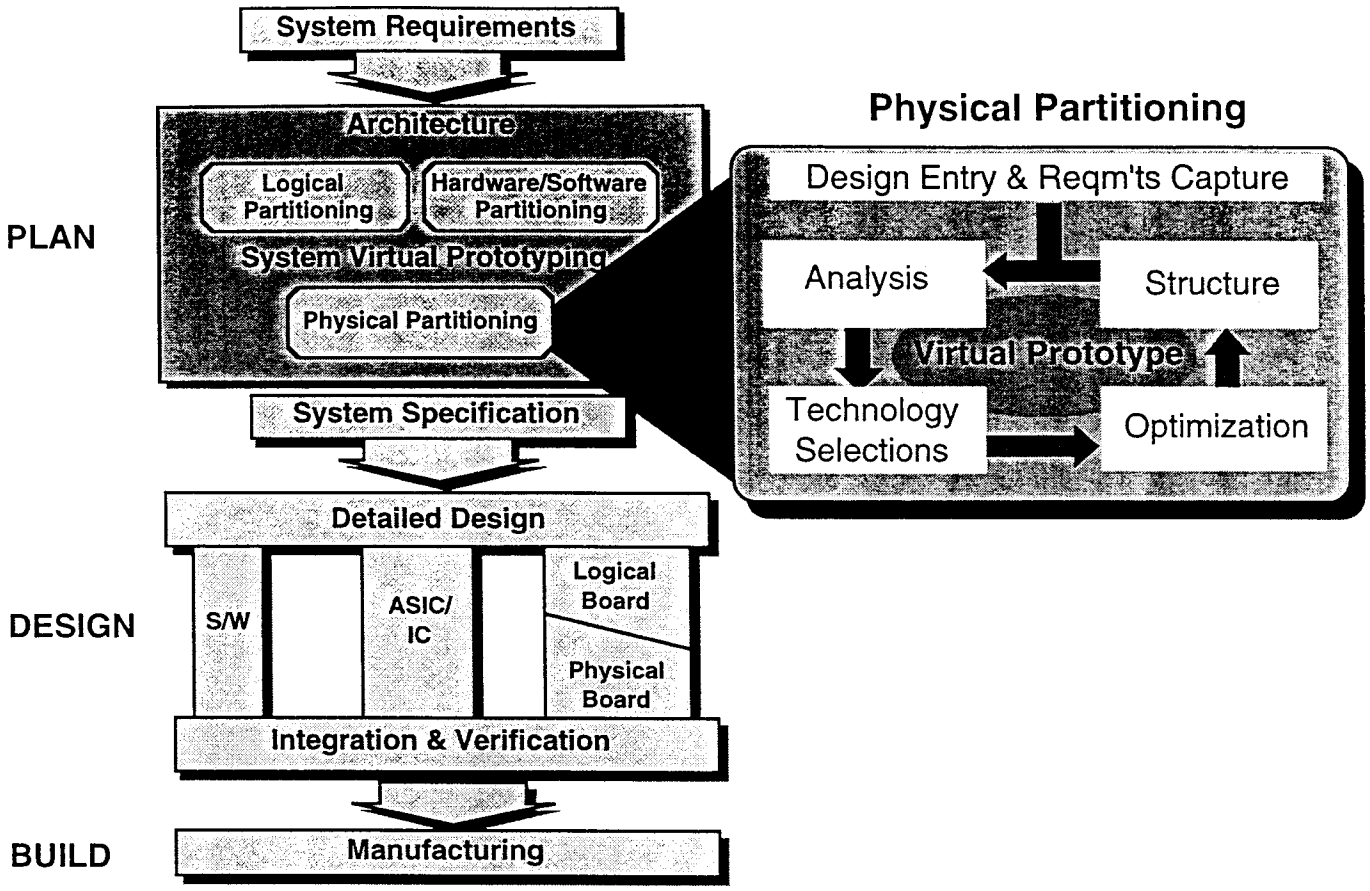

Figure 1 - System design flow using a system virtual prototyping methodology. The planning portion of the design flow is usually overseen by the "system architect" and implemented by the system designer using experts in ASIC synthesis, partitioning, and electronic packaging.

better" design requirements. They are the best choice for high performance systems, high density systems, and they accommodate very large silicon chips quite nicely. Unfortunately, the most dominant system driver is the need to make the electronic system "cheaper".

Therefore, today's system designer is faced with the fundamental tradeoff of advanced packaging vs. system cost. Since today's systems are extremely large and complex, choosing one implementation technology for the whole system is typically not the best answer. Optimizing the whole system for performance, results in wasted cost since even low performance sub-systems are implemented with expensive packaging technology. System designers today must choose the right technology for each portion of the system to optimize the size and performance characteristics against total system cost (Sandborn *et al*, 1996).

B. System Virtual Prototyping Design Flow

To deal with the fundamental system cost vs. advanced packaging tradeoff, the design flow shown in Figure 1 can be used. Figure 1 shows a system design flow starting with capturing the product requirements and ending with the delivery of the completed electronic system. The significant difference between this design flow and a typical flow used by system designers today is the addition of the system virtual prototyping activity.

System virtual prototyping is the creation of a model to analyze system characteristics prior to building the actual system or performing detailed CAD implementation tasks (layout, routing, verification, etc.). There are three major partitioning activities involved in creating this model. Hardware/Software partitioning is choosing which system requirements are met with software and which with hardware. Logical partitioning is determining which functionality goes in which chips, and physical partitioning is choosing the physical implementation structure of the hardware. Once the partitioning decisions are completed, the resulting system model can be analyzed against a variety of system requirements (functionality, size, speed, cost, design time, etc.). Assuming that all requirements are not met on the first attempt (usually a pretty good assumption), the virtual prototyping activity becomes an iterative process of changing system characteristics to optimally meet system requirements.

Most design methodologies today fall short primarily in the physical partitioning activity. Thorough analysis of the tradeoffs between a variety of implementation options is typically not done, and *ad hoc* decisions are made. The lack of a rigorous physical partitioning activity is due both to the lack of tools for performing these physical tradeoffs and to the lack of accurate manufacturing data to drive the tradeoffs. Poor tradeoff analysis creates a real problem in design because up to 80% of the system cost and performance becomes locked-in prior to the start of detailed system design. Attempting to make packaging and technology decisions later in the design process results in time consuming and costly redesign.

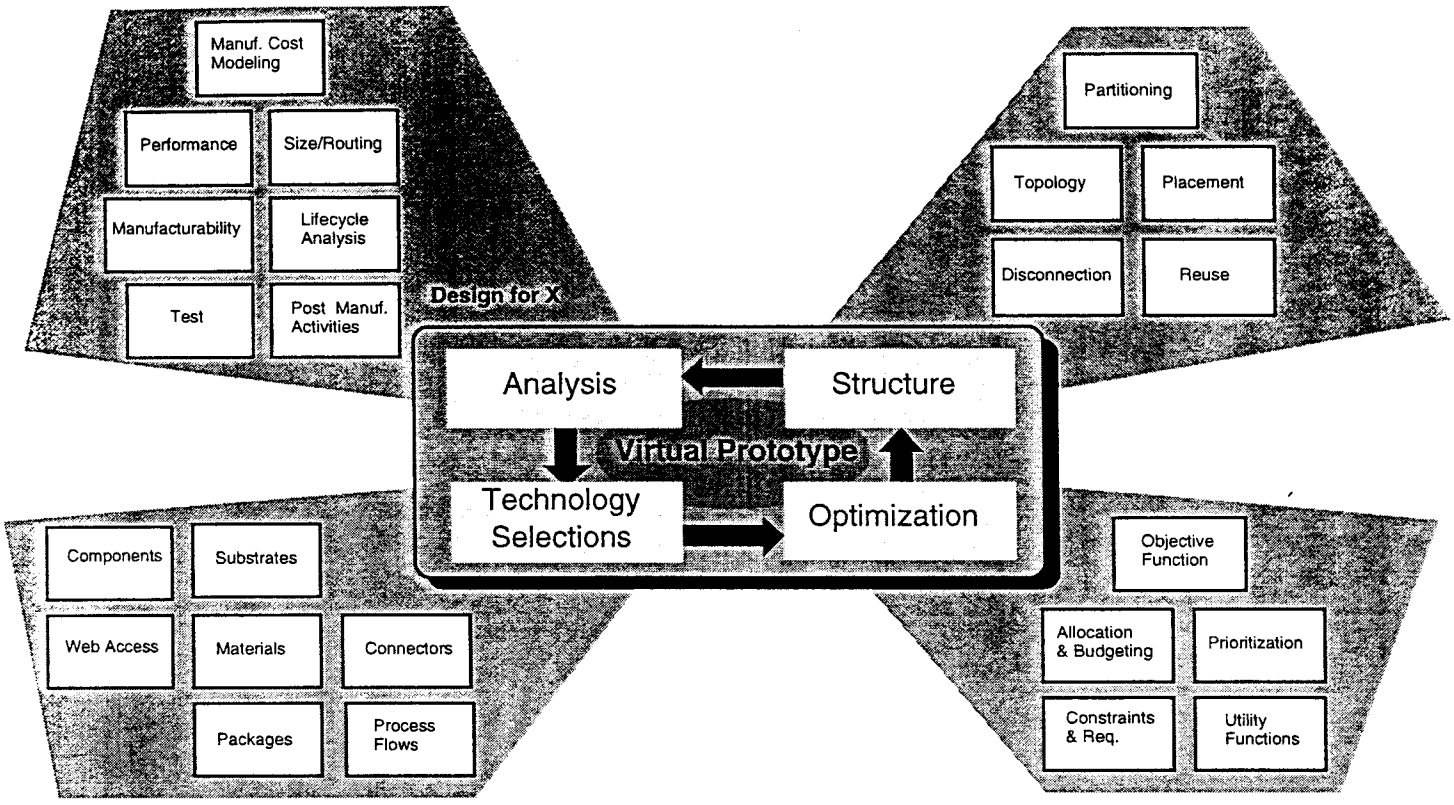

Figure 2 - Enabling activities (activity landscape) for system-level physical tradeoff analysis.

Historically, when there were fewer packaging and technology options available, the lack of rigorous analysis was not as much of a problem, since each design was similar to the previous one. Unfortunately with today's technology choices, it is not obvious which technology optimizes the cost of the system. Additionally, as the complexity of systems has grown, optimizing a system can no longer be accomplished by optimizing its parts, rather, the entire system must be considered during optimization. In Section III, an example is discussed that demonstrates the need for consideration of the whole system during optimization.

II. PHYSICAL PARTITIONING

System packaging decisions require a combination of activities associated with the structural definition of a system, quantitative analysis of the system's size/cost/performance, data support, and design optimization strategies. The physical partitioning analysis portion of the design flow presented in Figure 1 is expanded in Figure 2 to show the actual activity landscape associated system-level physical tradeoff analysis. Making decisions associated with how to optimally construct a MCM or when to insert a MCM into a system solely on the basis of electrical performance, or system size is very risky. The correct-by-design methodologies are based on an ability to make sound decisions prior to design implementation. Sound decisions require consideration of most, if not all, of the activities shown in Figure 2. In summary, failure to address all of the activities shown in Figure 2 may significantly limit the effectiveness and value of any single activity.

The landscape in Figure 2 consists of several interrelated parts:

Structure: Structure represents the physical architecture of the system. In the physical partitioning context, partitioning represents choosing the optimum number of packaging entities (MCMs, boards, etc.), and the best distribution of the candidate components among them. Reuse in this context implies modular partitioning[1]. One critical element of system-level physical partitioning is connection topological relationships (Wilson, 1982). The connection topology used has no relationship to the number of connections required, but will determine the number of interconnect crossovers (a crossover is created when one connection between modules or boards crosses over another). Crossovers tend to add complexity that penalizes the system's size, cost, reliability, and electrical performance. Closely related to topology is disconnection[2]. Disconnection is the methodology and physical realization of how separable physical entities are combined to form a system. Placement of components relative to each other within a physical entity is an important contributor to several performance measures including routability, electrical, thermal, and manufacturability.

Analysis: Analysis comprises all the "Design for X" activities (manufacturability, reliability, environment, testability,

[1] Maximizing the reuse of substructures over a single or multiple product space.

[2] Connecting objects together is easy. Connecting objects together under constraints that require the components to be disconnected (for upgradability, supportability, maintainability, testability, etc.) requires a different mind set. Therefore we refer to the activity of connecting components in a disconnectable fashion as the "Disconnection" problem.

design-to-cost, etc.) plus all performance estimation activities (electrical, thermal, etc.). This portion of the landscape can be populated with point design tools (simulators) and/or estimation-level advisors. Experience tends to indicate that most of the analyses performed in this area should lead back to cost at some level and must be tightly coupled to manufacturability. "Post Manufacturing Activities" include design for recyclability, disassembly, serviceability, maintainability, upgradability, etc. Lifecycle analysis (LCA) is a family of methods for systematically assessing material use, energy use, waste, services, processes and technologies over a product's entire life. Manufacturability addresses the ease with which a product can be manufactured and is usually accomplished via scorecarding or knowledge-base approaches.

Optimization: Optimization is a management framework within which all the partitioning and Design for X activities are performed. The optimization portion of the landscape shown in Figure 2 does not necessarily imply that the system must choose the optimum design specification without user involvement, but rather, it represents tools to aid the user in collaboratively optimizing their system's physical implementation.

Technology Selections: The volume of data that is potentially necessary for successful system tradeoff analysis can be significant. To complicate the problem, the necessary data is usually spread over both time and space, and standard information models for representing the data are not available for every type of technology needed. The ultimate solution to the data problem is a tradeoff analysis framework that electronically accesses the necessary data directly from the technology/component vendors during the tradeoff analysis process.

While many of the activities shown in Figure 2 do not exist today as formal methodologies or commercial software tools, the greatest discrepancy in populating the landscape are the lack of links between the Design for X activities and partitioning, and manufacturing knowledge. The most significant roadblock to realizing an integrated landscape is the lack of data access.

III. MCM SYSTEM DESIGN EXAMPLE

In this section, an example system design problem that includes a MCM is presented. The example highlights the need for considering the whole system and the inclusion of manufacturing knowledge during basic tradeoff analysis activities in order to accurately identify implementation opportunities that lead to more economical systems.

This example, considers systems implemented in MCM-L technology and was performed using the SavanSys Packaging Tradeoff Analysis tool (see Appendix). Interconnection of the systems in this example requires a board with eight layers. At the present time, it appears that for MCM-L substrates with less than or equal to eight layers, the least expensive board fabrication approaches are ones in which the vias are mechanically drilled (Figure 3). Above 8 layers, micro-via technologies, where the vias are fabricated using photolithography, plasma etching, or laser drilling appear to provide a less expensive approach.

The cost of fabricating a laminate board, is the cost of fabricating a laminate panel divided by the number of boards that fit on the panel (i.e., number-up). All mechanically drilled board fabrication technologies presently available, use material combinations and laminates that are not dimensionally homogeneous (i.e., during lamination they do not change shape the same way in the x direction as they do in the y direction). This requires that, for artwork compensation reasons, all the boards fabricated on the panel must be oriented in the same direction (homogeneous panelization). Some of the more expensive micro-via board fabrication approaches, however, can use materials (laminates) and constructions that are dimensionally homogeneous, thereby allowing boards to be arranged on the panel with varied rotations without artwork compensation problems. This in turn, presents the possibility that more boards can be fabricated on a panel. Figures 4 and 5 show results for this simple example.

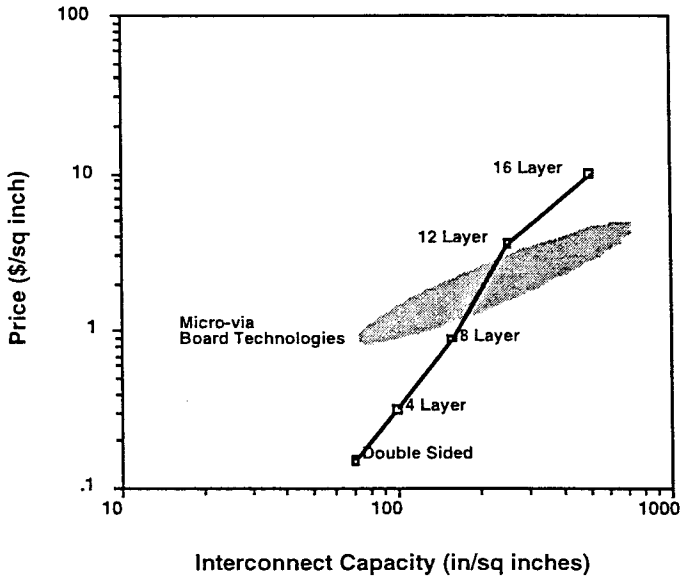

Figure 3 - Relative cost of conventional mechanically drilled laminate substrates and micro-via substrates (Fisher, 1996).

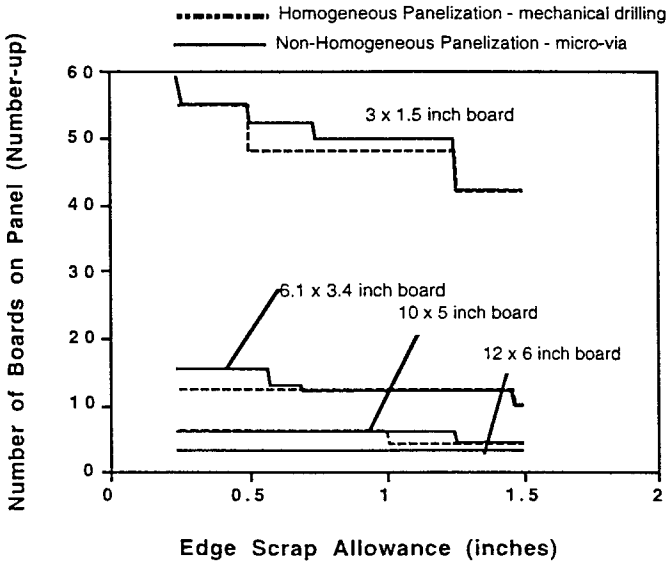

Figure 4 - Number of boards per 18 x 24 inch panel (number-up) as a function of the edge scrap allowance (amount of unused edge on the panel).

Figure 4 shows the number of boards that can be fabricated on a panel as a function of the amount of space needed around the edge of the board (edge scrap allowance). Algorithms for panelization appear in Sandborn *et al* (1997). Its obvious that for some board sizes and edge scrap allowances, no advantage is gained through non-homogeneous panelization, but in other cases the number of boards that can be fabricated on the panel increases. Figure 5 shows the cost per board corresponding to Figure 4. The results show that in at least one case, the more expensive micro-via approaches result in less costly systems because materials and manufacturability allow non-homogeneous panelization during manufacturing[3].

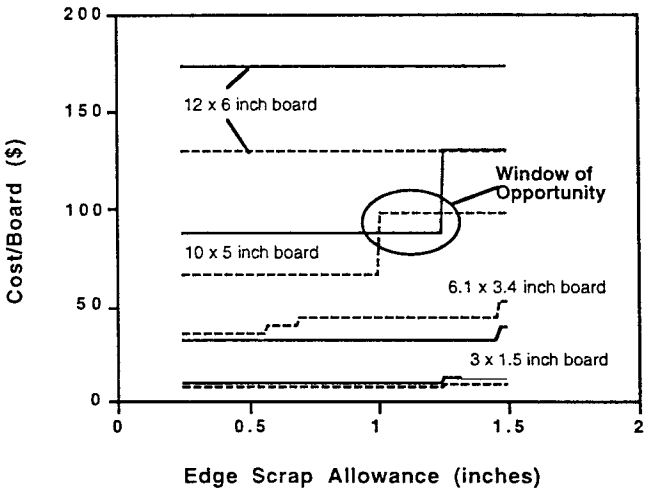

Figure 5 - Cost per board as a function of the edge scrap allowance. The "Window of Opportunity" marked on the graph shows, that depending on the board size and edge scrap allowance, there are conditions under which more expensive technologies can yield less expensive systems.

This example is a relatively straightforward application of manufacturing knowledge to basic technology tradeoff analysis, unfortunately, surprisingly few system designers consider simple manufacturability realities like panelization. Panelization is not "rocket science", but it does require that system designers have access to manufacturing knowledge.

IV. SUMMARY

This paper outlined a methodology called "System Virtual Prototyping" that brings analysis and optimization of basic packaging and physical partitioning tradeoffs to the front of the system design process. Combining accurate manufacturing information with design information to optimize the system characteristics is the central theme of the system virtual prototyping concept. Too often, system designers devote large resources to complex optimization exercises and through a failure to understand relatively simple manufacturing concepts miss much greater opportunities to improve their systems.

APPENDIX—THE SAVANSYS™ SYSTEM PACKAGING TRADEOFF TOOL

SavanSys is a software tool for enhancing the manufacturability and decreasing the design risk associated with the selection of packaging technologies for integrated circuits. The SavanSys software tool performs system packaging tradeoff analysis. SavanSys concurrently computes physical (size, weight, interconnect routing requirements, escape routing), electrical (delays, attenuation, dc drops, effective inductance), thermal (internal and external thermal resistances, air cooling), reliability (MTTF), and cost/yield performance metrics for multichip systems.

The SavanSys tool focuses on the physical partitioning portion of the virtual prototyping methodology shown in Figure 1. SavanSys currently accommodates all the activities shown in Figure 2 with the exception of the optimization activities.

Multichip modules (MCMs) and traditional packaging (through-hole and surface mounting) technologies treated by SavanSys include: traditional and fine-line printed circuit boards, low temperature cofired ceramic, and thin-film (chip-first and chip-last). Component assembly approaches include wirebonding, TAB, flip chip, and single chip packages. Materials are also available for bare die attach, encapsulation, attaching extrusions, and for defining the bonding and substrate technologies.

SavanSys provides the user the ability to compute the cost of assembled electronic systems, including component costs, component preparation (wafer and die level burn-in, bumping), single chip package costs, surface mount and through-hole assembly costs, bare die attach costs (TAB, wirebond, flip chip), tooling costs associated with the processes above, substrate costs, repair and rework costs, and test costs. In addition, learning curves may optionally be defined for any or all steps in the process, and handling costs may be defined for all steps that involve the insertion of components into the process flow.

The SavanSys tradeoff analysis tool is specifically designed to allow the impact of technology, material, and design rule variations on the cost and performance of a board or system of boards. SavanSys enables designers to make optimum physical implementation and physical partitioning choices early in the design process to facilitate successful implementation decisions. SavanSys is integrated into the Mentor Graphics and Cadence physical design frameworks and is compatible with Aspect and DIE format databases.

[3] This analysis ignores potential system density improvements (i.e., layer reduction) that may also be possible with micro-via technology.

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