A comparison of routing estimation methods for microelectronic modules

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Abstract
It is often necessary to estimate the number of board layers in electronic modules before detailed routing is possible. Several methods for estimating board interconnect requirements prior to the existence of a netlist have been developed. Some estimation approaches depend on the use of heuristics derived from studying actually routed designs, while others depend on geometric or statistical arguments. The applicability and uncertainties associated with these estimation techniques are not widely understood. In this paper several different routing estimation methods are applied to a variety of printed wiring board and multichip module applications. The accuracy with which the methods predict the amount of required wiring is compared.

Introduction

One of the drivers of an electronic system's size and cost is the amount of wiring resources available within a board. System designers must be able to predict the wiring utilization of electronic systems during the earliest stages of the design process, i.e. during virtual prototyping (Sandborn and Vertal, 1998). Unfortunately, actual routings require the development of netlists and pin placement information; neither of these items are generally available in the early stages of conceptual design; therefore, routing estimation approaches play an important role during technology tradeoff analyses.

The goal of routing estimation is to predict the required design rules and number of wiring layers necessary to realize a design within specified size constraints, or alternatively to determine that wiring is not a size limiting constraint for a specific application.

The goal of this paper is to compare several existing routing estimation methods and address their applicability and uncertainties.

Routing estimation methods

This section provides brief descriptions of the routing estimations compared in this paper. Since a paper many times the length of this one would be required to derive the methods used, only high-level summaries are provided here. More detailed descriptions and derivations can be found in the references (Sutherland and Oestreicher, 1973; Landman and Russo, 1971; Bakoglu, 1990; Donath, 1974; Hannemann, 1994; Moresco, 1990; Seraphim, 1977; Coors *et al.*, 1990).

Several definitions are helpful for the discussion that follows. A net is a group of two or more pins (chip I/O or I/O leaving the module) that are electrically connected together. An interconnect is a single point-to-point connection. A net is made up of one or more interconnects. The fanout of a net is one less than the number of pins a net connects together. The number of interconnects in a net is equal to its fanout. The interconnect capacity (also called the connectivity) is a measure of the amount of wiring available in a board. A common description of interconnect capacity is the available length of wiring per unit area of the board (e.g. inches/square inch). Parallelism is a measure of the number of nets that follow similar paths (i.e. nets that go from equivalent drivers to equivalent receivers). If there are a large number of parallel nets, the parallelism is "high".

The methods discussed in this section are generally formulated to compute routing limited board area. The number of wiring layers (N_w) required is embedded in the interconnect capacity (I_c), which is the product of the number of wiring layers and the interconnect capacity per layer. Alternatively, all the formulations can be recast to solve for N_w for a specified board area.

Section-crossing approach (Sutherland and Oestreicher, 1973)

The wiring limited size of a board, or alternatively the number of wiring layers, may be determined by estimating the number of connections that must pass through various board cross-sections.

Let P_1 and P_2 represent the fraction of signal pins on each side of an arbitrarily drawn cross-section of a board so that $P_1 + P_2 = 1$; the section need not divide the board in half.

For randomly chosen nets, the probability that a wire crosses a section of the board at least once is given by

$$P_c = 1 - P_1^n - P_2^n \quad (1)$$

where

n = the average number of pins per net (i.e. the fanout + 1)

P_1^n = the probability that the wire starts on side 1 and connects only to pins on side 1 (i.e. never crosses the section).

The number of wires that cross the section is the probability of crossing multiplied by the total number of nets in the system (N_{io}/n),

$$W = \frac{N_{io}}{n}(1 - P_1^n - P_2^n) \quad (2)$$

where N_{io} is the total number of I/O to be routed together in the system. Since W is a maximum when $P_1 = P_2 = 1/2$, the worst case length of the section is then given by

$$L = \frac{W_{max}}{F_i I_c} \quad (3)$$

where I_c is the interconnect capacity and F_i is the wiring efficiency (fraction of the wiring capacity that can actually be used for interconnection).

In order to obtain the board size one should consider a minimum of two perpendicular cross-sections. The off-module connections can be accounted for by considering the module under analysis to be part of a larger board with the number of off-module connections equaling the number crossing between the module under analysis and the phantom larger board.

Requirements versus resources approaches

The second class of routing estimation approaches is based on setting the resources available for wiring equal to the wiring requirements of the chips.

The total wire length that can actually be used is given by

Resources (total wiring length available for use) = $\text{Area} F_i I_c$ (4)

where

F_i = fraction of the available wiring that can be used (governed by the complexity of the routing problem and the quality of the router).

Microelectronics International
17/1 [2000] 36–41

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I_c = interconnect capacity, function of the design rules on the wiring layers and the number of wiring layers.
Area = board area.

If the chip set being considered is homogeneous (all the chips have the same size and number of I/O) then the board area is given by Area = $N_{chip}F_p^2$ where N_{chip} is the number of chips in the module and F_p^2 is the wiring limited footprint of one of the chips (where the board connector is treated as a chip included in the routing).

Several methods for computing the routing requirements have been developed. The following four subsections represent alternative methods of determining the routing requirements.

A. Rent's rule approach (Landman and Russo, 1971)

A number of efforts have focused on the estimation of average interconnect length based on parametric models of real wiring data. The total wiring length required to connect a set of chips is given by Bakoglu (1990)

Requirements (total wiring length required) =

$$\frac{f}{f+1}N_{io}L_{avg} \tag{5}$$

where
f = average fanout of a chip's I/O.
N_{io} = total number of I/O in the system (all the chip I/O plus all the I/O going off the module).
L_{avg} = average interconnection length in the board, $L_{avg} = R_mF_p$.
F_p = wiring limited chip footprint dimension
R_m = average interconnect length in units of F_p.

The critical activity associated with this method is the determination of R_m. Donath (1974) derived a Rent's Rule based formula for an upper bound on expected average interconnection length based on partitioning results for linear and square arrays of gates. This formulation takes into account, to first order, the effect of placement on distance. Bakoglu (1990) applies Donath's result for the chip level to the module level. By replacing the number of gates with the number of chips and the gate pitch with the chip wiring limited footprint dimension, F_p, the average interconnect length at the board level in units of F_p is given by,

$$R_m = \frac{2}{9}\left(7\frac{N_{chip}^{-0.5}-1}{4^{-0.5}-1} - \frac{1-N_{chip}^{-1.5}}{1-4^{-1.5}}\right)\frac{1-4^{-1}}{1-N_{chip}^{-1}}, \quad (\beta \neq 0.5) \tag{6}$$

where β is the Rent's exponent, a measure of the parallelism in the structure to be interconnected.

To determine the wiring limited chip footprint, F_p, or the number of wiring layers required in the board, set (4) equal to (5) and solve for F_p or N_w.

B. Hannemann's approach (Hannemann, 1994)

Hannemann's approach depends on a dimensionless quantity H, given by

$$H = \frac{bN_{io}}{L\sqrt{N_{chip}}} \tag{7}$$

where
b = feature size parameter = W_p or $V_p/(T_c+1)$
W_p = wiring pitch
T_c = the number of tracks
V_p = via pitch
L = board dimension
N_{io} = number of signal and control I/O in the system
N_{chip} = number of chips in the system.

H is related to the number of layers (N_w) in a board by a factor c (N_w = cH). An appropriate value of c was determined by fitting a plot of N_w versus H for many known boards. Using this method, Hannemann suggested the use of a value of 3.9 for c. The board area predicted by this method can be found by solving for L^2.

C. Geometric approach (Moresco, 1990)

The geometric method is based on a requirements equals resources argument similar to Bakoglu's approach, but is not Rent's Rule based, rather it is an extended neighbor counting based method similar in concept to Seraphim (1977). In the geometric approach, the wiring requirement is computed by assuming that a fraction of the nets (A) are routed only to their nearest neighbor routed and the rest of the nets (1-A) are globally routed, and the total required wire length is given by,

Requirements (total wiring length required) =

$$A\frac{N_{chip}N_{io_e}F_p}{2} + (1-A)(N_{chip}-1)N_{io_e}F_p + \frac{N_{io_e}F_p\sqrt{N_{chip}}}{v} \tag{8}$$

where,
N_{io_e} = the number of signal and control I/O per chip
N_{io_e} = the number of signal and control I/O leaving the module
v = 2 for edge connector and 4 for an area array connector on the bottom of the board
A = fraction of nets that are nearest neighbor routed ($0 \bullet A \bullet 1$)
N_{chip} = number of chips in the module
F_p = wiring limited chip footprint dimension.

The parameter A is a measure of parallelism in the system. A = 1 is maximum parallelism and A = 0 is the minimum. To determine the wiring limited chip footprint, F_p, or the number of wiring layers required in the board, set (4) equal to (8) and solve for F_p or N_w.

D. Statistical wire length distribution approach (Coors et al.*, 1990)*

This method is based on a probability distribution of interconnect lengths. This method derives an expectation value for the interconnect lengths in a board,

$$E = \frac{1}{a}\left[\frac{(S-T)(Sa-2)e^{aS} + S(2-(S-T)a)e^{a(S-T)} - 2T}{(S-T)e^{aS} - Se^{a(S-T)} + T}\right. \tag{9}$$

where
S = M + N
$T = \sqrt{M^2+N^2}$
M = $\frac{\text{length}}{G}+1$ and N = $\frac{\text{width}}{G}+1$
length, width = length and width of the board
G = pad placement grid size, derived from the board area, total number of I/O, and packaging density; or the bond pad pitch averaged over all components in the module
a = ln α where α is an empirically derived constant between 0 and 1, suggested value = 0.94.

The total length of wire required is found from the product of the number of interconnects and the length of each interconnect,

required length of wiring = $\frac{f}{f+1}N_{io}GE$. (10)

To determine the wiring limited chip footprint, F_p, or the number of wiring layers required in the board, set (4) equal to (10) and solve for F_p or N_w.

All of the approaches discussed in this section, in their simplest form, assume that the component set is homogeneous (i.e. all the components are the same), which is rarely a good approximation to real world problems. It is important to note that this restriction appears at two critical points:

1 the derivation of the wiring capacity limited footprint; and
2 the determination of the overall board size.

One approach to addressing this problem is to compute a unique effective number of homogeneous chips (and a corresponding average interconnect length) for each component. The simplest way to compute a new effective number of chips is from the ratio of the number of signal connections in the whole module and the number of signal connections that the ith component has,

$$N_{chip_i} = \frac{\text{Number of signal connections in the whole module}}{\text{Number of signals connections in the component of interest,}} \quad (11)$$

and the board area is not the product of F_p^2 and the number of chips, but a summation of the form, $\sum_{i=1}^{N_{chip}} F_{p_i}^2$.

Comparison of estimation methods

In this section we compare the accuracy of the routing estimation methods for several designs. The first subsection describes the comparison process, and the second subsection provides results for several more example boards.

Analysis process description

One common attribute of all the estimation methods is their dependence on one or more calibration factors. Each of the estimations can yield reasonable results for real systems if its calibration factor(s) are set appropriately, the difficulty is knowing how to set the calibration factors. To assess the accuracy of the routing methods, each method was used to predict the wiring resources required by a sample design as a function of the calibration factor(s). The metric used for assessing the accuracy of the methods was total etch length. The total etch length is the total length of wiring required to route the design and is a readily available output from actual routing activities.

The example case that we will use to demonstrate the analysis process is a microprocessor printed wiring board incorporating ASICs, MPU, glue logic, and memory that was presented in Coors *et al.* (1990) (additional details about the board appear in Case 1 in Table I). Figures 1-5 show the estimated wiring results for this example. The line labeled "Actual" in all the Figures represents the total wiring length used in an actual routing of the board (1,323 inches for this example).

Figure 1 shows the results of the Rent's Rule routing analysis. In the Rent's Rule case, the calibration factor is the Rent's exponent, β. Bakoglu (1990) suggests using a default value of 0.6 for Rent's exponent when treating module-level problems. For this example case, the performance of the Rent's Rule model using the $\beta = 0.6$ is very good, resulting in an error of 7.6 percent in predicted wiring length. The calibration factor in the Geometric model is the ratio of nearest neighbor to globally routed nets, A. Figure 2 shows that the Geometric model underpredicts the required wiring length for all possible values of A for this example case. In general, the Geometric model works best for modules that have a high degree of parallelism (which this example does not). In the Hannemann method, the calibration factor is the slope of the N_w versus H relation, c. Figure 3 shows that the value of c must be approximately 1.4 in order to accurately predict the wiring required by this example. The Hannemann approach is most accurate for cases in which N_w is large (i.e. $N_w > 8$) and does not generally yield accurate results for problems with small N_w or H.

Figure 1
Rent's Rule routing estimation results. Default value of β suggested by Bakoglu is 0.6

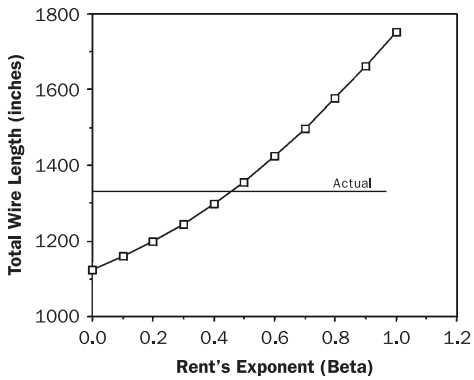


Table I
Example board characteristics

Case	Components	Signal I/O*	Quantity	Number of signal nets	Number of off-board signal I/O*	Actual total wire length (inches)	Routable area (square inches)
1 Microprocessor PWB	See Coors *et al.*	1394	57 chips 58 discretes	407	100	1323	18.75
2 Crossbar Switch	VLSI	284	37	7,188	4,164	17,475	36
3 Microprocessor module	VLSI	281	4	637	688	1,622	5.06
	MSI	140	2				
4 Crossbar switch	VLSI	84	16	637	304	602	6.25
	Other	15	6				
5 Microprocessor module with cache memory	SRAM	20	20	291	104	549	6.25
	VLSI1	259	1				
	VLSI2	124	1				
	Buffer	5	2				
	Discretes	70 total	48				
6 Microprocessor module with cache memory	CPU	152	1	251	102	441	2.94
	Cache cont.	245	1				
	SRAM	30	8				
	Resistor	1	8				
7 Data storage/ accumulator module	A/D convert	6	8	74	80	18.75	0.64
	A/D convert	22	1				
	Op amps	10	2				
	Resistor	2	8				

Note: * Signal I/O refers to signal and control I/O

Figure 2
Geometric routing estimation results

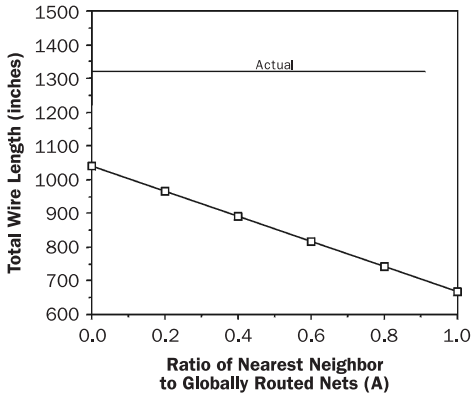


Figure 3
Hannemann model routing estimation results. Default value of c suggested in Hannemann is 3.9

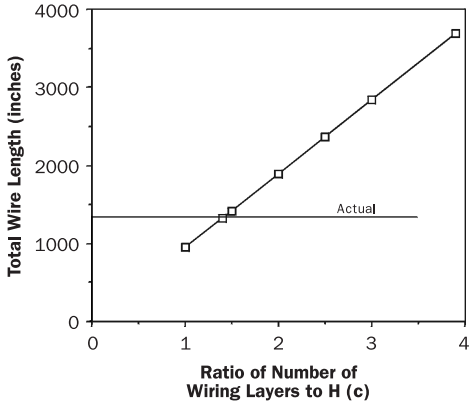
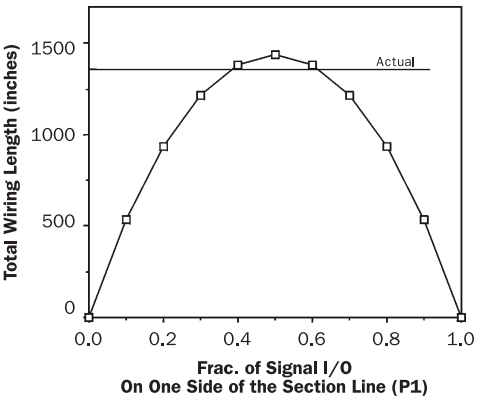


Figure 4
Section-crossing routing estimations results



The calibration factor in the section-crossing model is the fraction of I/O on one side of the section line (P_1 or P_2). In this comparison approach we have only computed the length of a single cross-section of the board (assumed that the area of the board is the length of that section squared). The section-crossing method shown in Figure 4 returns reasonable results for this example case (P_1 = 0.5, overestimates the total wire length by 8.6 percent).

Figure 5
Statistical wire length distribution model results. Default value of α suggested in Coors *et al.* (1990) is 0.94

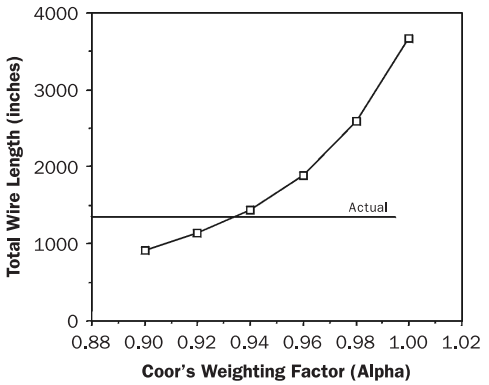


Figure 5 shows the results using the statistical wire length distribution method where the calibration factor is the value of α. The method overestimates the wiring length needed by 8.3 percent when using the 50mil pad placement grid size used in the actual routing.

Before addressing the performance of the various methods on specific problems, we should point out that different methods are appropriate for different applications. For example, Coors *et al.* (1990) state that the statistical wire length distribution method is not appropriate for designs with highly parallel interconnect structures that are typical for designs with a significant percentage of memory chips. Hannemann's method (Hannemann, 1994) is appropriate for interconnect structures with high layer counts and relatively course line pitch. Sutherland and Oestreicher (1973) indicate that the section-crossing method is only applicable in cases where random placement assumptions are reasonable. Alternatively, the two most widely used methods, Rent's Rule and the Geometric approach, can be adapted to a wider range of applications because they can be adjusted to compensate for the amount of parallelism required to interconnect a given design. The Geometric method is based upon a measure of the number of nets that interconnect with adjacent neighbors versus more distant chips. For a design with a high degree of parallelism, a large fraction of the interconnect would be connected to a nearest neighbor. As a result, this method can be useful for a wide range of designs. Likewise, Rent's method requires that a measure of parallelism be provided in order to calculate the average interconnect length.

Summary of example results

In this subsection we have included routing estimation analysis results for several examples. Table I shows the board characteristics and actual routing statistics for the example set of designs and Table II shows a summary of the routing estimation results for the example designs described in Table I.

Rent's Rule provided the closest estimation in four of the seven cases (1, 3, 6 and 7) shown in Table II for β = 0.6 (this value of β indicates a moderate amount of parallelism). For the four cases listed above, the average error was 16 percent. However, case 7 is different from the other three cases in that the vast majority of the signal connections run directly between the module I/O and the chip I/O rather than between chips as is the situation with the other three cases. When case 7 is ignored, the average error drops to 6 percent. Cases 1, 3 and 6 are microprocessor modules with associated memory chips. Thus Rent's Rule method for β = 0.6 appears to be appropriate for this type of application. It should be

Table II
Summary of routing estimation results for the example cases described in Table I

Case	Actual wire-length (inches)	Rent's rule β = 0.6 Est.	Error	Geometric* Est.	Error	Hannemann c=3.9 Est.	Error	Section-crossing P_1 = 0.5 Est.	Error	Statistical wire length distribution α = 0.94 G = 50mils Est.	Error
1 Microprocessor PWB	1,323	1,423	0.08	1041 A = 0	–0.21	3,689	1.79	1,437	0.09	1433	0.08
2 Crossbar switch	17,475	13,129	–0.24	17,895 A = 1	0.021	40,996	1.34	22,242	0.27	1,1742	–0.33
3 Microprocessor module	1193	1,149	–0.04	1357 A = 0	–0.14	13,653	10.44	1,074	–0.10	1,366	0.15
4 Crossbar switch	602	946	0.57	708 A = 1	0.18	2,966	3.93	1,000	0.66	782	0.30
5 Microprocessor module with cache memory	549	375	–0.31	547 A = 1	0.003	3,393	5.18	582	0.06	801	0.46
6 Microprocessor module with cache memeory	441	467	0.06	335 A = 1	–0.24	2,042	3.63	321	–0.27	482	0.09
7 Data storage/ accumulator module	18.75	28	0.47	40 A = 1	1.13	97	4.12	31	0.64	66	2.5

Note: * The value presented is where the closest correlation occurred

noted that for case 2, the Rent's Rule method predicted the actual wire length within 5 percent with $\beta = 1$. This value of β is typical for a structure with extreme parallelism such as a crossbar switch like case 2. In case 6, the error ranged from 4 percent to 9 percent for respective values of β between 0.1 and 1.0, indicating a very weak dependence on parallelism. If an additional complexity coefficient were used to modify R_m according to the complexity as a function of component placement, suitable results are obtainable for a wider range of cases.

The Geometric approach provided the closest estimation for three cases (2, 4 and 5). Cases 2 and 4 are crossbar switches while case 5 is a microprocessor module with 20 memory chips; all of these structures have a very high degree of parallelism. For these three cases, the average error was approximately 7 percent. All three cases had the best correlation to the actual results when A = 1 (maximum parallelism) which is appropriate.

The Hannemann method is appropriate for interconnect boards with high (> 8) layer counts and coarse pitches. For all of the modules analyzed in this paper, the error when compared to the actual requirements was very large. However, none of the cases considered in this paper fits the characteristics that we would expect to be accurately treated by the Hannemann approach.

A key assumption in the section-crossing approach is that of random placement (i.e. a change in any component's placement is expected to have no effect on the average interconnect length in the board). The better a system approximates to this condition, the better the section-crossing model will predict its wiring requirements. In cases that are highly parallel (like crossbar switches), the section-crossing model should significantly overpredict the amount of wiring required as seen in cases 2 and 4. In cases that better approximate random placement (low degree of parallelism) the section-crossing model should more accurately predict the resources necessary as in cases 1 and 3. In case 7 (the few chip package case), observing the actual module layout and routing results indicates that a high percentage of the routing is from component I/O to board I/O (not from component to component); therefore, very few nets actually cross through any cross-sections that divide the board. As a result the section-crossing model overpredicts the length of wire needed by a large amount.

Based upon the modules evaluated in this study, the statistical wire length distribution method is appropriate for applications where the average bond pitch is in the range of 40-50mils, typical for many printed wiring boards (PWB) that are designed for surface mount assembly. Case 1, a PWB with peripheral leaded surface mount technology, provided the closest estimation of the actual requirements.

Summary and conclusions

It should be stressed that all of the methods considered in this paper are applicable to some class of applications. In some cases the class of applications is more narrowly defined than others, and some of the methods are more universally applicable than others. The following paragraphs summarize the findings in this paper.

In this study, the Rent's Rule and Geometric methods provided the closest correlation between estimated and actual routing requirements. For modules with a balanced mixture of random and parallel interconnect, the Rent's Rule method with B = 0.6 provided a very accurate prediction (± 6 percent). For modules with extremely high parallelism, the Geometric method with A = 1 provided an equally accurate prediction (± 7 percent).

The Geometric method with A = 1 provides an accurate prediction for highly parallel structures with fine pitch interconnect such as with thin film interconnects. Hannemann's method was not suitable for the low layer count, fine pitch boards used in the applications described in this paper. The section-crossing method modeled cases with low parallelism with reasonable accuracy but significantly overpredicted the wiring needed by highly parallel cases. The statistical wiring distribution approach appears to be an accurate method for predicting the wiring requirements of printed wiring board/SMT applications; however, a priori prediction of the appropriate value of the pad placement grid size is not straightforward.

The results presented in this paper are preliminary. Many more cases need to be studied in order to draw definitive conclusions about the applicability of the routing estimation methods.

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