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## A REVIEW OF THE ECONOMICS OF EMBEDDED PASSIVES
**(EXTENDED ABSTRACT)**

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### ABSTRACT
This paper provides an overview of the economic issues and cost models associated with the conversion of discrete passives to embedded passives in printed circuit boards. Three attributes of economic analysis are included herein: fabrication and manufacturing cost analyses, embedded resistor trim and rework economics, and non-manufacturing life cycle costs that are impacted by the conversion of discrete passives to embedded passives. In addition, a complete set of references to existing work on the economics of embedded passives is provided.

### INTRODUCTION
Economics encompasses an assessment of the total life cycle cost of a design decision where the life cycle includes the design, manufacturing, testing, marketing, sustainment, and end-of-life of the product. The decision to convert discrete passives to embedded passives is much further reaching than simply reducing the cost of part procurement and paying more for the board. In addition, there are a host of other cost and benefit issues to be considered that translate into life cycle economics at some level. This paper reviews the economic attributes of a system's design and production that impact the decision to use embedded passives and outlines existing models for addressing economic tradeoffs.

Embedded passives are fabricated within substrates and, while embedded passives will never replace all passive components, they provide potential advantages for many applications. The generally expected advantages include:

- Increased circuit density through saving real-estate on the substrate
- Decreased product weight
- Improved electrical properties through additional termination and filtering opportunities, and shortening electrical connections
- Cost reduction through increasing manufacturing automation
- Increased product quality through the elimination of incorrectly attached devices
- Improved reliability through the elimination of solder joints.

Potentially the biggest single question about embedded passives is their cost, "…of all the inhibitors to achieving an acceptable market for integral substrates, the demonstration of cost savings is paramount" [1]. There is considerable controversy, however, as to whether applications fabricated using embedded passives will ever be able to compete economically with discrete passive technology. On the bright side, the use of embedded passives reduces assembly costs, shrinks the required board size, and negates the cost of purchasing and handling the discrete passive components that are replaced. However, these economic advantages must be traded off against the higher cost (per unit area) of boards fabricated with embedded passives (a situation that will not disappear over time) and possible decreases in throughput and yield of the board fabrication process.

The application-specific costs depend on many effects when embedded passives are present in a board:

- Decreased board area due to a reduction in the number of discrete passive components
- Decreased wiring density requirements due to the integration of resistors and bypass capacitors into the board
- Increased wiring density requirements due to the decreased size of the board
- Increased number of boards fabricated on a panel due to decreased board size
- Increased board cost per unit area
- Decreased board yield
- Decreased board fabrication throughput

- Decreased assembly costs
- Increased overall assembly yield
- Decreased assembly-level rework.

Several other recurring system costs may also be affected by the use of embedded passives, for example: the need to electromagnetically shield the board may be reduced or eliminated when certain passives are embedded (saving on expensive materials and their assembly), and the costs associated with thermal management of the board may also be affected.

Due to the opposing nature of many of the effects listed above, the overall economic impact of replacing discrete passives with embedded passives is not trivial to determine and, in general, yields application-specific guidelines instead of general rules of thumb. In fact the very nature of tradeoff analysis is one in which *the greater the detail necessary to accurately model a system, the less general and more application-specific the result*.

## FABRICATION AND MANUFACTURING COST MODELING

Several previous works have addressed cost analysis for embedded passives and thus provide varying degrees of insight into the economic impact of embedded passives. The target of all these economic analyses is to determine the effective cost of converting selected discrete passive components to embedded components. The most common approach to economic analysis of embedded passives is to: 1) reduce the system cost by the purchase price and conversion costs[1] associated with the replaced discrete passives, 2) reduce the board size by the sum of the layout areas associated with the replaced discrete passives and determine the new number of boards on the panel, and 3) determine the new board cost based on a higher per unit area cost for the embedded passive panel fabrication and the new number-up computed in step 2. The results of these three steps determine the new system cost.

Brown [2] presents an outline of all the potential contributions to the life cycle cost of embedded passives. Rector [1] provided the economic analysis using the first-order approach outlined above. Ohmega Technologies Inc. has also generated a cost model for assessing cost tradeoffs associated with its Ohmega-Ply® embedded resistor material, [3]. The Ohmega cost model follows the first-order approach described above, and includes yield and rework effects. Realff and Power, [4], developed a technical cost model for board fabrication and assembly associated with embedded resistors. The model includes test (board and assembly), yield, and rework. Power *et al.* [5] extend the model in [4] to embedded capacitors and cast it in the form of an optimization problem targeted at choosing which discrete passives to integrate based on an assumption of assembly and substrate manufacturing process details, and material properties.

Another analysis that recently appeared focused on design tradeoffs for a GPS front end, [6]. This analysis includes detailed cost modeling of thin-film embedded resistors and capacitors performed using the Modular Optimization Environment software tool from ETH, [7].

A recent manufacturing cost model from Sandborn *et al* [8], includes the analyses performed in the previously referenced models and incorporates quantitative routing estimation and assesses board fabrication throughput impacts for setting profit margins on board fabrication, effects that have not been included in previous models. This model, outlined in Figure 1, is a very good example of a complete manufacturing/ fabrication tradeoff analysis model for embedded passives. The model works in the following way:

1. Accumulate the area of the footprints of discrete passives to be embedded.
2. Reduce board area by the accumulated discrete passive area from step 1 maintaining the aspect ratio of the original board. This step is optional, i.e., the board area may be fixed.
3. Plated or Printed Resistors: Determine the area occupied by each plated or printed embedded resistor on wiring layers. Perform routing analysis removing nets and vias associated with resistors that are embedded and accounting for area blocked by embedded resistors on wiring layers. Routing is assumed to be unaffected by discrete resistors embedded using Ohmega-Ply® or similar dedicated layer addition approaches. Bypass Capacitors (distributed capacitors): All nets and vias associated with embedded bypass capacitors are removed from the routing problem. Singulated Capacitors: Assume that embedded singulated capacitors do not affect routing analysis. Using these assumptions determine the relative change in routing resources due to embedding selected passives.
4. Using the layer requirements, the relative routing requirements for the embedded substrate and either a fixed measure of the routing efficiency associated with the conventional board or a range of possible efficiencies determined under the assumption that the conventional version of the board did not include any more layer pairs than it needed to route the problem, compute the number of required layer pairs for the embedded passive implementation.
5. Determine the yield of layer pairs that include embedded passives.
6. Determine the trimming cost for embedded resistors. The necessity of trimming is determined by the resistor's tolerance. The application-specific cost per trim is determined by modeling the throughput of a laser trimming process, [9].
7. Compute the number of boards per panel from the board size (number-up) and the effective panel fabrication costs from the layer and material requirements, yields, and resistor trimming costs.
8. Determine the relative board fabrication profit margin from layer pair throughput modeling. A profit margin model based on throughput is provided in [8], and throughput is modeled in [10].
9. Accumulate assembly cost, test, rework, and board fabrication costs (with profit margin) to obtain total relative cost.

[1] Conversion costs are the handling, storage and assembly costs associated with a discrete component.

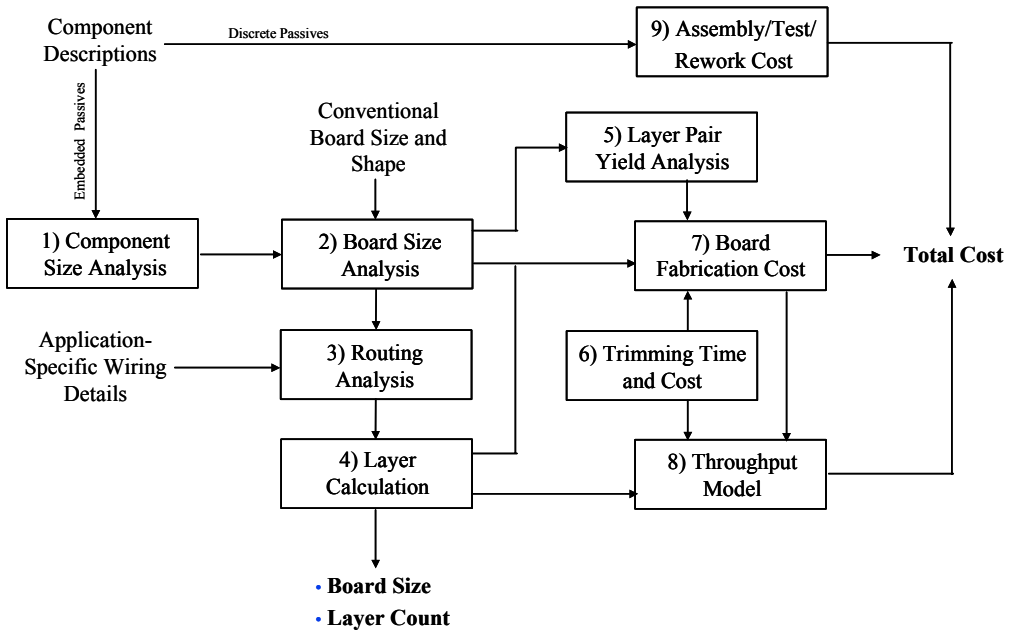


Figure 1 – Embedded passive board cost tradeoff model [8].

The analysis in Figure 1 focuses on differences in system cost between embedded passive and discrete passive solutions, therefore all cost elements that are approximately equivalent for the embedded and conventional system are effectively igonored, e.g., all functional testing of the system and, procurrement and assembly costs associated with non-embeddable parts.

## EMBEDDED RESISTOR TRIMMING AND REWORK ECONOMICS

Laser trimming of film resistors has been performed for many years. For many applications (depending on design tolerances) embedded resistors will need to be trimmed. Resistors are trimmed by machining a trough in the resistive element, the length and path-shape of which determine the resistance change obtained, [11].

It is also possible to consider reworking embedded resistors prior to completion of the board fabrication process. Resistors may be reworked because their initial value is too large due to either trimming errors or original fabrication (trimming can only increase the resistance of a resistor). One method of reworking embedded resistors is to print conductive ink on the surface of an embedded resistor thus adding a lower value parallel resistor that effectively "trims down" the resistor value, [12].

A cost of ownership model for a laser trimming process has been developed by ESI, [9]. The ESI model allows the amount of time to trim a layer pair to be computed as a function of the number of resistors to be trimmed per layer pair and the size of the panel (laser trimming throughput). A version of the ESI model is used in the analysis process shown in Figure 1 (Step 6).

Unfortunately, trimming and rework equipment is expensive and both processes potentially represent bottlenecks in the board fabrication process. Therefore, the question that arises is, under what conditions (application properties and resistor fabrication process) is it economically feasible to perform trimming and possibly rework versus disposal of layer pairs or boards that do not meet design specifications?

When resistors are fabricated the resulting values form a distribution, Figure 2. If the resistors are to be trimmed, the fabrication target resistance (peak of the distribution) is below the application target resistance so that the greatest number of fabricated resistors can be trimmed to values in the specified range. The High Specification Limit (HSL) and the Low Specification Limit (LSL) are determined from the design tolerance associated with the resistor. The area under the curve between the HSL and the LSL represents the yield of the

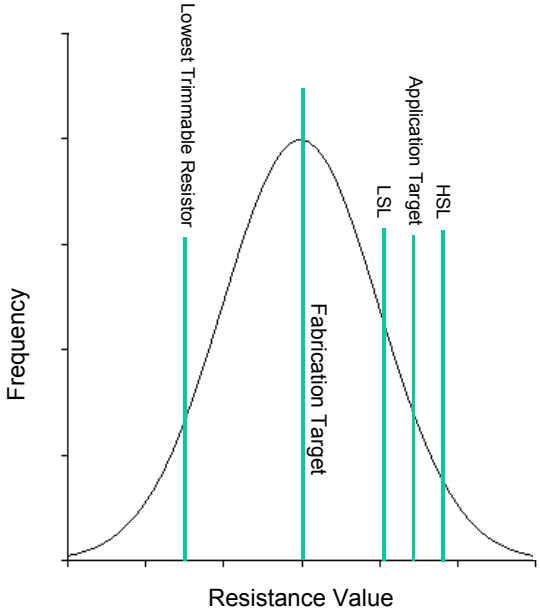


Figure 2 – Distribution of fabricated resistor values.

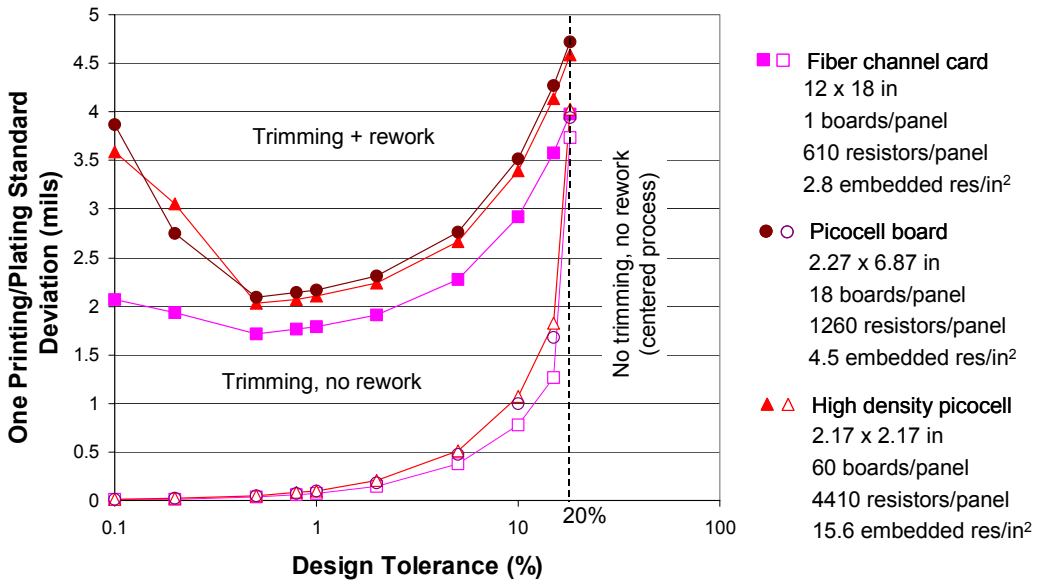


Figure 3 – Application-specific economical regions of trimming and reworking embedded resistors. This example result assumes no resistor thickness variation, see [13] for additional assumptions and modeling parameters associated with this result.

untrimmed resistor. There is a lower limit to the ability to successfully trim a resistor that is approximately 55% of the application target. The area between the lower trimming limit and HSL represents the yield of trimmed resistors (assuming no trimming defects). Resistors in the distribution that have values below the lower trimming limit or above HSL would generally be considered yield loss (unusable and untrimmable). Rework allows resistors above HSL to be recovered and used. In cases where no trimming is planned, the process would be centered so that the fabrication target and the application target are the same.

Figure 3 shows the result using the model developed in [13] for three different applications. The three regions identified in Figure 3 provide the conditions, under which it is most economical to trim, trim and rework, and simply scrap non-conforming inner layer pairs.

## LIFE CYCLE COSTS IMPACTED BY EMBEDDED PASSIVES [14]

Thus far we have only considered system manufacturing issues. This only represents a portion of the economic impacts of converting discrete passives to embedded passives. Life cycle effects, which for many applications will dominate manufacturing costs, include all other activities associated with the product. Generally speaking, life cycle effects are more difficult to quantify into costs than manufacturing activities. Life cycle activities that will be impacted by embedded passives include:

Design Costs – Costs of engineering and other technical personnel to design boards that include embedded passives. If designers require specialized training, or new CAD and/or other specialized design tools to successfully perform embedded passive board design, then the costs of these activities must be considered. A summary of the design tool requirements for embedded passives is included in the NEMI 2002 Industry Roadmap, [15]. One must also consider costs associated with effort and tools for design verification and functional test development. Extra design costs may also include libraries of models for embedded passives ranging from symbol libraries to high-performance RF models for use in electrical simulation. The inclusion of embedded passives may also affect the degree to which a design can be reused and upgraded (re-design costs). Also included in the design costs are prototyping costs. Are embedded passive applications going to require additional prototype boards?

Non-Recurring Costs – To what extent will embedded passives require board fabricators to invest in new equipment (see [4] for an equipment analysis)? Equipment is not the only non-recurring cost that may be associated with embedded passives. There will be additional tooling (artwork) for layer pair production, potentially additional chemistry to be managed in the board fabrication process, and finally licensing fees and royalties may have to be paid for the use of technology, material, and/or processes.

Time-to-Market – Does the design, verification, and prototyping of embedded passive boards require more calendar time than that for conventional systems? Delays in time-to-market for a new product of weeks or months can cost substantial money and in some cases mean missing the market for the product completely.

Performance Value – Embedded passives may result in size or performance improvements in a system that enable increases in market share for the manufacturer. It may be the case that for some quantifiable increase in system cost, a manufacturer can differentiate itself from its competition by providing a product that is lighter, smaller, faster, more reliable, or with greater functionality than its competition, and the customer is willing to pay extra for one or more of these improvements.

Qualification and Certification – The introduction of new materials and processes into board fabrication requires material providers and board fabricators to assess and possibly update safety certifications, e.g., UL Certification. While the cost of this type of certification is not directly borne by the users of embedded passives, it will be reflected in the board costs. On the other hand, there will be a reduction in the costs associated with qualifying discrete component manufactures.

Liability – Embedded passives, or any new technology, material, or process may carry with it unforeseen financial liabilities. The liabilities may be in the form of causing injury to customers, employees of the manufacturer, or the environment. Long-term studies of the effects of the materials and the processes used to incorporate them into boards may be necessary to prove or disprove liability claims.

Sustainment – Sustainment is a collection of many activities all of which have an economic impact. In general, sustainment is all the activities necessary to:

- Keep an existing system operational (able to successfully complete the purpose it is intended for);
- Continue to manufacture and field versions of the system that satisfy the original requirements;
- Manufacture and field new versions of the system that satisfy evolving requirements.

The foremost concern with embedded passives is reliability. Conventional wisdom is that system reliability will improve because of the reduction in the number of solder joints, however, this will only be realized if the reliability does not commensurately decrease due to other embedded passive specific effects. Reliability questions arise from two origins: first are the specific embedded structures as reliable or more reliable than the rest of the components and packaging? Secondly, are there embedded passive specific processing conditions (during board fabrication) that remove life from other conventional board structures? Changes in system reliability appear either as warranty costs (replacement) or as maintenance costs (repair).

For systems that are subject to repair, embedded passives may change the ease with which problems in the system can be diagnosed, physically repaired and retested. In turn, if the faulty board is to simply be replaced, its reliability impacts the number of "spare" boards that must be manufactured to fulfill expected replacement commitments.

Sustainment, however, goes further than reliability driven replacement and repair. Sustainment also means that the system should remain manufacturable through the end of its support life (to fulfill additional requirements for new product and spare replenishment). This is not generally difficult for manufacturers of laptop computers and other short-life consumer products, but is a huge concern (and cost issue) for long-life products such as avionics for aircraft. The biggest component related problem that long field life systems see is obsolescence (particularly electronic part obsolescence), [16]. Most electronic parts have short lifetimes (from an availability perspective) relative to even the design cycle of an aircraft, let alone an aircraft's support life. For systems like aircraft, qualification and certification requirements may make simple substitution for obsolete parts with newer parts prohibitively expensive. Embedded passives will mitigate some obsolescence problems by replacing discrete parts that would become obsolete. On the other hand, if the materials used to manufacture the embedded passives within the board become obsolete, i.e., replaced by newer materials, the overall obsolescence problem may well become much worse. Models for the application-specific economic impact of part obsolescence appear in [17].

Environmental and End of Life – The fabrication of passives within boards obviously increases the volume of waste produced during the board fabrication process. Disposition of board fabrication waste is a significant contributor to the price of boards. If any of the embedded passive specific contributions to the waste steam are considered hazardous then the waste disposition costs could increase. Waste disposition is also a factor at the other end of the life cycle, i.e., at end-of-life. Depending on the type of product that the embedded passive board is being used within and the location in the world where the product is being sold, the manufacturer may bare some or all of the cost of disposing of the product when the consumer has finished with it.

Financial – Several costs associated with creating and holding inventory (handling, storage, procurement) associated discrete passives are potentially avoided, this includes the cost of money that is invested in stored passives as opposed to invested elsewhere.

## SUMMARY

An overview of cost modeling efforts associated with embedded passives has been provided. Extensive example analyses performed with the models discussed in this paper are available in the references, e.g., [8] and [14]. It can not be overstressed that the opposing nature of many of the effects associated with embedding passives in printed circuit boards makes the overall economic impact of replacing discrete passives with embedded passives a non-trivial economic tradeoff to perform and that application-specific analyses need to be performed to determine the economic viability of such a conversion.

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