

A New Test/Diagnosis/Rework Model for Use in Technical Cost Modeling of Electronic Systems Assembly

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Abstract

This paper presents a test/diagnosis/rework analysis model for use in technical cost modeling of electronic assemblies. The approach includes a model of test operations characterized by fault coverage, false positives, and defects introduced in test, in addition to rework and diagnosis operations that have variable success rates and their own defect introduction mechanisms. The model can accommodate an arbitrary number of rework attempts on any given assembly and can be used to optimize the fault coverage and rework investment during system tradeoff analyses.

The model's implementation allows all inputs to the model to be represented as probability distributions thereby accommodating inevitable uncertainties in input data present during tradeoff activities and uses Monte Carlo methods to determine model outputs.

1. Introduction

At a fundamental level, electronic system design is a tradeoff analysis activity with uncertain inputs. This tradeoff includes factors such as size and performance, but often the most important factor in the tradeoff is cost. The various costs that affect the manufacture of the system are the fabrication or assembly cost, test/inspection cost, rework cost, and waste disposition cost. In addition, there are significant non-manufacturing life cycle costs associated with system sustainment, end-of-life, and other issues. Of the manufacturing costs, the test and the rework costs can be very important drivers that significantly affect the total cost of manufacturing for many products. Modeling the test/diagnosis/rework costs accurately may determine the extent to which the system designer can control and optimize the manufacturing cost.

Technical cost modeling (e.g., [1], [2]) is one method that is useful for economic tradeoff analysis. Technical Cost Modeling (TCM) is defined as a process-based, "bottoms-up" approach to cost estimation, with total cost broken into a set of individual cost elements

(process steps). Each of these elements is estimated separately, and then summed to provide an estimate of the total cost. Thus, the complex task of cost estimation is reduced to a set of simpler algorithms, which can be estimated based on science, engineering, accounting, or expert judgment. The modeling of a process flow (sequence of process steps) is central to TCM, [3].

The goal of TCM is to understand the overall and component costs of a product and how these costs change when product and/or process changes are made. Specifically, this includes dividing cost into its constituent components: variable cost elements, which includes materials, labor, and utility; and the fixed cost elements, which includes equipment, tooling, maintenance, and the cost of capital. Once these costs are established, sensitivity analysis can be performed to understand the impact of changes to key parameters like annual production volume, process yield, throughput and tooling cost.

Consequently, a detailed test/rework model, which includes diagnosis and the effects of factors like false positives and defects introduced by the test, diagnosis, and rework, which can be included within technical cost models is a critical component necessary for design tradeoff analysis.

The context that interests us in this paper is electronic board assembly. In board assembly the tradeoff problem addressed is: at what point(s) in the process do I stop and test, how much test (fault coverage) do I pay for at those point(s), when in the process do I rework, and how many attempts do I make to rework before scrapping a defective assembly? The answer to these questions is application specific necessitating a comprehensive test/diagnosis/ rework model for use in tradeoff analysis.

The next section of this paper outlines the existing test/rework models that can currently be used with technical cost modeling. Section 3 describes the new model developed by the authors. Section 4 demonstrates the new model by providing example results.

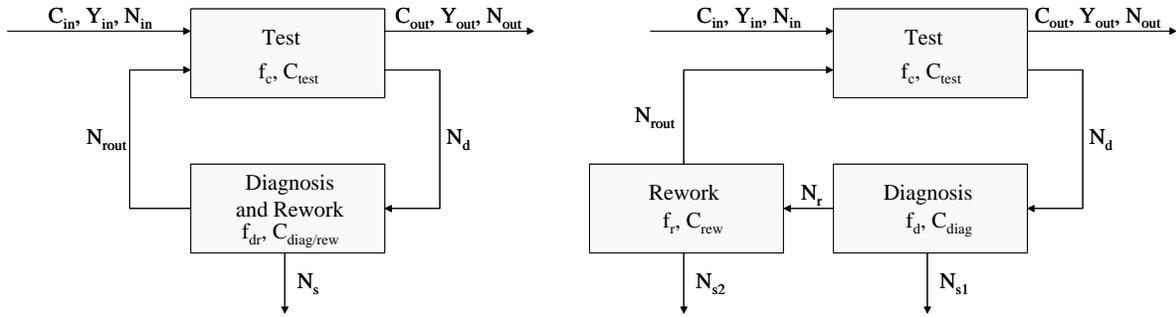


Figure 1 – Example test/diagnosis/rework models currently in use for technical cost modeling. C = cost, Y = yield, N = number of parts, f_c = fault coverage, f_{dr} = fraction of parts that are diagnosable and reworkable, f_r = fraction of parts that are reworkable, f_d = fraction of parts that are diagnosable, and N_s = number of parts scrapped.

2. Existing Models

There are several existing test/rework models that are applicable to TCM. The basic test/rework models, that are currently in use, are shown in Figure 1. In the example test/diagnosis/rework models shown in Figure 1 all parts coming from production are tested; the diagnosis and repair are applied to all the parts that are identified as defective during the test; and all reworkable parts are retested. Many versions of these models supporting some subset of the variables shown have been developed including single rework attempt models and multiple rework attempt models [4]-[10]. Although the detail accommodated in these models varies, in general they do not account for new defects introduced during the test, diagnosis or rework processes; false positives in testing, or uncertainties in the input data.

In order to accommodate the additional effects and obtain a model that is readily useable in a technical cost modeling environment, we have formulated the new more comprehensive test/diagnosis/rework model that is discussed in the next section.

3. Detailed Test/Diagnosis/Rework Model

The objective of the new test economics model is to accommodate the test/diagnosis/rework effects relevant to printed circuit board fabrication and electronic system assembly processes. In these processes, defect insertion during test and rework operations is not uncommon (e.g., from handling and/or probes making physical contact with the board), false positives¹ can be a significant problem especially in board fabrication, multiple rework attempts are made when dealing with

¹ A false positive is a positive test result in subjects who do not possess the attribute for which the test is conducted.

expensive systems such as multichip modules, and complex rework operations that may include reassembly of significant portions of the system are performed.

Figure 2 shows the content of the new test/diagnosis/rework model. In the following description we use the word “part” to refer to the item being tested (e.g., a board assembly). Inputs to this model are the accumulated cost and yield of upstream processes (C_{in} and Y_{in}), N_{in} is not a required input and is included for convenience in the formulation of the model.² The test portion of the model is the top most group of three steps. This model can be used to account for defects introduced by the test operation both prior to the actual test (e.g., loading the part into the tester or stationing the probes on the part) and after the test result is recorded (e.g., unloading the part from the tester). The parts that are determined to be faulty go on to the diagnosis step. Three outcomes are possible from diagnosis: 1) no fault is found in which case the part goes back for retesting, 2) the part is determined to be reworkable and sent on to rework, or 3) the part is determined to be non-reworkable and sent to scrap. The rework process operates on the reworkable parts and scraps parts that can not be successfully reworked. The reworked parts are re-tested and if the reworked parts are found to be faulty again, the parts are again sent for diagnosis. This rework process can be performed a fixed number of times (attempts). The new model simultaneously considers the effect of fault coverage and false positives on the cost and yield.

² In general yield and cost results from this model are independent of N_{in} , however, if equipment, tooling, or other non-recurring costs are included, the results become dependent on N_{in} and can be computed from accumulations of time specific equipment is occupied or the quantity of tooling used to produce a specific quantity of parts, see equations (18)-(20) and associated discussion.

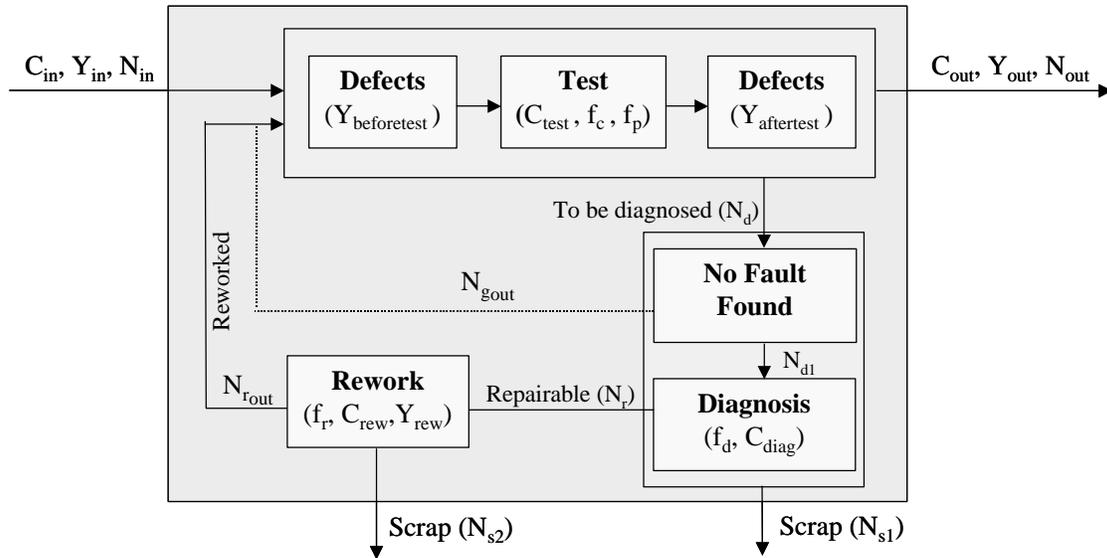


Figure 2 – Organization of the new test/diagnosis/rework mode. Table I describes the symbols appearing in this figure.

Table I – Nomenclature used in Figure 2 and throughout the discussion in this paper.

C_{in}	Cost of a part entering the test/diagnosis/rework process	N_{in}	Number of parts entering the test/diagnosis/rework process
C_{test}	Cost of test/part	N_d	Total number of parts to be diagnosed
C_{diag}	Cost of diagnosis/part	N_{gout}	Number of no fault found parts
C_{rew}	Cost of rework/part (may be a computed quantity, see Section 4.2)	N_{d1}	$N_d - N_{gout}$
C_{out}	Effective cost of a part exiting the test/diagnosis/rework process	N_r	Number of parts to be reworked
f_c	Fault coverage	N_{rout}	Number of parts actually reworked
f_p	False positives fraction, or the probability of testing a good part as bad	N_{s1}	Number of parts scrapped by diagnosis process
f_d	Fraction of parts determined to be reworkable	N_{s2}	Number of parts scrapped during rework
f_r	Fraction of parts actually reworked	N_{out}	Number of a parts exiting the test/diagnosis/rework process, includes good parts and test escapes
Y_{in}	Yield of a part entering the test/diagnosis/rework process	<div style="border: 1px solid black; padding: 5px;"> Versions of C_{in}, Y_{in} and N_{in} appear both with and without subscripts in the preceding discussion. When the variables appear with out subscripts they refer to the values entering the process. When they have subscripts, they represent specific rework attempts. </div>	
$Y_{beforetest}$	Yield of processes that occur entering the test		
$Y_{aftertest}$	Yield of processes that occur exiting the test		
Y_{rew}	Yield of the rework process (may be a computed quantity, see Section 4.2)		
Y_{out}	Effective yield of a part exiting the test/diagnosis/rework process		

There are several assumptions made in the formulation of this model:

- Defects introduced by the diagnosis step are not explicitly treated.
- False positive (f_p) and fault coverage (f_c) act simultaneously and they are independent of each other, i.e., the fault coverage acts only on bad parts and the false positive acts either only on good parts or on all parts.

The cost incurred by all the parts that eventually pass the test step is given by,

$$C_1 = \sum_{i=0}^n (C_{in_i} + C_{test}) N_{out_i}, \quad (1)$$

where n is the number of rework attempts allowed, i.e., the maximum number of attempts to rework an individual part is n and N_{out_i} is number of parts passed by the test in the i^{th} rework attempt (see (8) and associated discussion). When $i=0$, C_1 is the total cost of the parts that pass the test without ever going through diagnosis or rework. The cost incurred by all the parts scrapped by the diagnosis step is given by,

$$C_2 = \sum_{i=1}^n (C_{in_i} + C_{test} + C_{diag}) N_{s_{1i}}, \quad (2)$$

and the cost incurred by all the parts scrapped by the rework step is given by,

$$C_3 = \sum_{i=1}^n (C_{in_i} + C_{test} + C_{diag} + C_{rew}) N_{s_{2i}}, \quad (3)$$

where $N_{s_{1i}}$ and $N_{s_{2i}}$ are defined in (10) and (11). After the final rework (n^{th} rework attempt), the parts that do not pass the test are scrapped. The first term in (4) accounts for the defective parts scrapped by the final test, and the second term accounts for any false positives that are encountered during the final test,

$$C_4 = N_{d_{n+1}} (C_{in_n} + C_{test}) + N_{in_n} Y_{in_n} Y_{beforetest} f_p (C_{in_n} + C_{test}) \quad (4a)$$

when f_p applies to only good parts, and

$$C_4 = N_{d_{n+1}} (C_{in_n} + C_{test}) + N_{in_n} f_p (C_{in_n} + C_{test}) \quad (4b)$$

when f_p applied to all parts.

N_{in_n} appearing in (4) is defined in (13). The total cost of all the parts (including scrapped parts) is the sum of C_1 through C_4 . The total effective cost per output part associated with this model is the total cost divided by

the total number of output parts (parts that are eventually passed by the test),

$$C_{out} = \frac{C_1 + C_2 + C_3 + C_4}{N_{out}}. \quad (5)$$

The treatment of the false positives affects both the number of parts moving through the process and the yield of those parts. The test step is characterized by both fault coverage and false positives (f_p = probability of testing a good part as bad which should not be confused with the escape fraction which is the probability of testing bad parts as good). Let us assume that the false positives are created by the test before the identification of faults. Let the number of parts that come into the test affected by the false positives be N_1 and the yield coming in be Y_1 . Let the number of parts going out (after false positives are created) be N_2 and their yield be Y_2 . These parts consist of both good (g) and bad parts (b) such that $N_1 = N_{1g} + N_{1b}$ and $N_2 = N_{2g} + N_{2b}$, Figure 3.

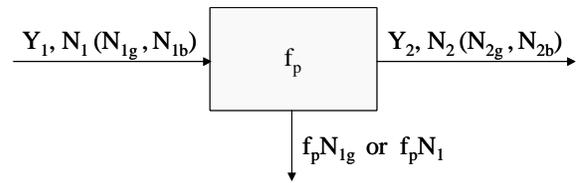


Figure 3 – Notation for false positive formulations.

There are several approaches to modeling the affect of the false positives. If we assume that the number of false positives sent to diagnosis by the test step will be $f_p N_{1g}$ based on the assumption that false positives only act on good parts. The false positive fraction is given by,

$$f_p = \frac{N_{1g} - N_{2g}}{N_{1g}} \quad (6a)$$

$$Y_2 = \frac{N_{2g}}{N_2} = \frac{(1-f_p)N_{1g}}{(N_1 - f_p N_{1g})} = \frac{(1-f_p)Y_1}{1-f_p Y_1}. \quad (7a)$$

An alternative assumption is that the number of false positives sent to diagnosis by the test step will be $f_p N_1$ based on the assumption that false positives act on all parts.³ The false positive fraction is given by,

³ In this case, the false positives can be created from already defective parts, i.e., defective parts are detected as defective by the test step for the wrong reasons.

$$f_p = \frac{N_1 - N_2}{N_1} \quad (6b)$$

$$Y_2 = \frac{N_{2g}}{N_2} = \frac{(1-f_p)N_{1g}}{(1-f_p)N_1} = \frac{N_{1g}}{N_1} = Y_1, \quad (7b)$$

in other words, f_p in this case reduces the good and bad parts proportionately thus leaving the yield unchanged.

The number of parts moving through the process are shown in (8)-(13),

$$N_{out_i} = N_{in_i} \left(1 - f_p Y_{in_i} Y_{beforetest}\right) \left(\frac{(1-f_p)Y_{in_i} Y_{beforetest}}{1-f_p Y_{in_i} Y_{beforetest}}\right)^{f_c} \quad (8a)$$

$$N_{dl_i} = N_{in_i} (1 - f_p Y_{in_i} Y_{beforetest}) - N_{out_i} \quad (9a)$$

when f_p applies to only good parts, and

$$N_{out_i} = N_{in_i} (1 - f_p) (Y_{in_i} Y_{beforetest})^{f_c} \quad (8b)$$

$$N_{dl_i} = N_{in_i} (1 - f_p) - N_{out_i} + f_p N_{in_i} (1 - Y_{in_i} Y_{beforetest}) \quad (9b)$$

when f_p applied to all parts.

$$N_{s1_i} = (1 - f_d) N_{dl_i} \quad (10)$$

$$N_{s2_i} = (1 - f_r) N_{r_i} \quad (11)$$

$$N_{r_i} = f_d N_{dl_i} \quad (12)$$

$$N_{in_i} = \begin{cases} N_{in} & \text{when } i = 0 \\ f_r N_{r_i} + f_p N_{in_{i-1}} Y_{in_{i-1}} Y_{beforetest} & \text{when } i > 0 \end{cases} \quad (13)$$

where parameters without subscripts (N_{in} , C_{in} , and Y_{in}) indicate values entering the process (Figure 2) and the form of (8) follows from [11]. The total number of parts that successfully pass the test process is given by,

$$N_{out} = \sum_{i=0}^n N_{out_i} \quad (14)$$

The part counting in (8)-(13) assumes that all false positives on good parts go through diagnosis and back into test without scrapping of parts in diagnosis or rework. The formulation is also only valid when $f_p < 1$, $Y_{in} > 0$ and $Y_{beforetest} > 0$. The input cost (C_{in_i}) that appears in (1)-(4) is given by C_{in} when $i = 0$ and by (15) when $i > 0$.

$$C_{in_i} = \frac{(C_{in_{i-1}} + C_{test} + C_{diag}) f_p Y_{in_{i-1}} Y_{beforetest} N_{in_{i-1}}}{N_{in_i}} + \frac{(C_{in_{i-1}} + C_{test} + C_{diag} + C_{rew}) f_r N_{r_{i-1}}}{N_{in_i}} \quad (15)$$

The input yield (Y_{in_i}) that appears in (4) and (8)-(15) is given by Y_{in} when $i = 0$ and by (16) when $i > 0$.

$$Y_{in_i} = \frac{f_p Y_{in_{i-1}} Y_{beforetest} N_{in_{i-1}} + Y_{rew} f_r N_{r_{i-1}}}{N_{in_i}} \quad (16)$$

The final yield of parts that successfully pass the process is given using the general result in [11], [12], by,

$$Y_{out} = \frac{\sum_{i=0}^n Y_{aftertest} N_{out_i} \left(\frac{(1-f_p)Y_{in_i} Y_{beforetest}}{1-f_p Y_{in_i} Y_{beforetest}}\right)^{1-f_c}}{N_{out}} \quad (17a)$$

when f_p applies to only good parts, and

$$Y_{out} = \frac{\sum_{i=0}^n Y_{aftertest} N_{out_i} (Y_{in_i} Y_{beforetest})^{1-f_c}}{N_{out}} \quad (17b)$$

when f_p applied to all parts.

Note, N_{in} cancels out of (5) and (17) making the total cost per part and final yield independent of the number of parts that start the process, which is intuitively correct since no volume-sensitive effects (such as material or equipment costs) are included in the model so far.

In order to support the calculation of equipment costs associated with the test, diagnosis and rework activities, the total time spent in each activity can be accumulated. The effective tester, diagnosis, and rework time per part can be formulated using (8)-(13),

$$T_{total\ test} = \frac{T_{test}}{N_{out}} \sum_{i=0}^n N_{in_i} \quad (18)$$

$$T_{total\ diag} = \frac{T_{diag}}{N_{out}} \sum_{i=1}^n (N_{dl_i} + B) \quad (19)$$

where

$$B = \begin{cases} f_p N_{in_i} Y_{in_i} Y_{beforetest}, & \text{when } f_p \text{ applies to only good parts} \\ f_p N_{in_i}, & \text{when } f_p \text{ applies to all parts} \end{cases}$$

$$T_{\text{total rew}} = \frac{T_{\text{rew}}}{N_{\text{out}}} \sum_{i=1}^n N_{r_i} \quad (20)$$

where T_{test} , T_{diag} , and T_{rew} represent the equipment times for individual parts.

Dick *et al.* [13] point out that one of the main drawbacks in using economics models in general, and specifically for making test strategy decisions using economics models, is arriving at misleading results because of inaccurate inputs. To accommodate uncertainties in input data, the model has been implemented within a Monte Carlo analysis framework similar to that in [13]. Each non-integer input can have a designated distribution type (triangular distributions are used as an example in Section 4). Random numbers are used to select values from the distributions with which to perform the analysis. When a sufficiently large sample size has been completed, histograms of the output parameters can be created and mean and standard deviations of the solutions determined.

The model discussed in this paper is being used within several technology tradeoff analysis software tools and cost analysis tools. For testing and tutorial purposes, a standalone version of the model has been implemented in the web-based Java applet shown in Figure 4.

4. Example Results

This section presents example results generated using the model discussed in Section 3 and the application of the model to an electronic power module.

4.1 Example Results

The baseline data used for the first example in this section is given in Table II. The results in this section are presented in terms of yielded cost. Yielded cost is defined as cost divided by yield. In electronic assembly, yielded cost represents the effective cost per good (non-defective) assembly for a manufacturing process [14].

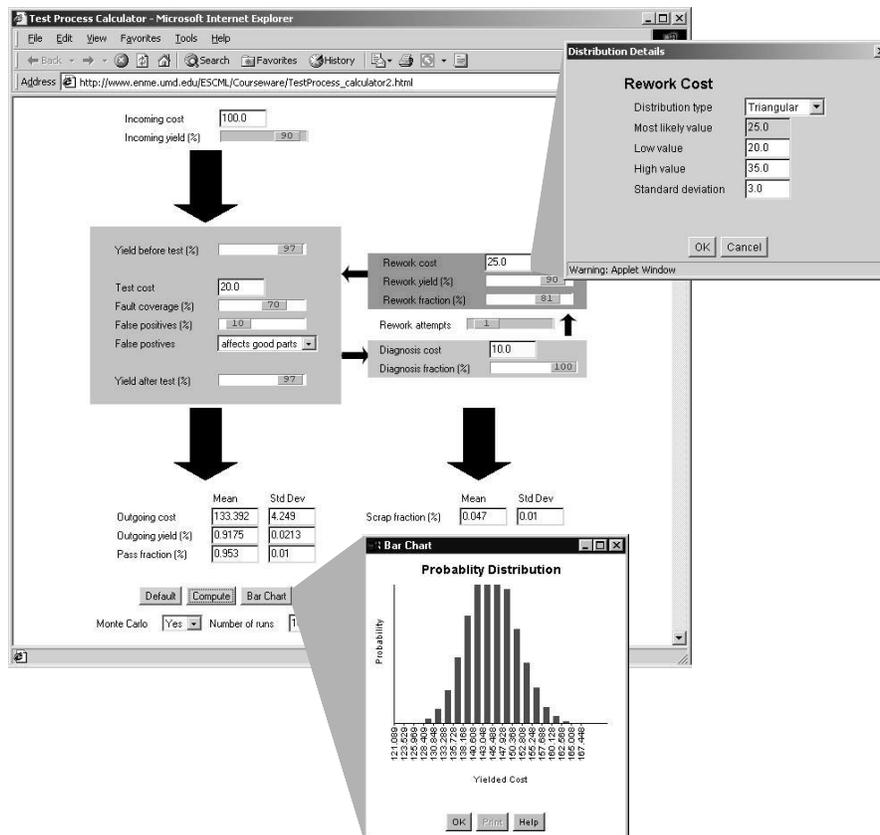


Figure 4 – Web-based interface for the model discussed in this paper (www.enme.umd.edu/ESCML/Courseware/TestProcess_calculator2.html).

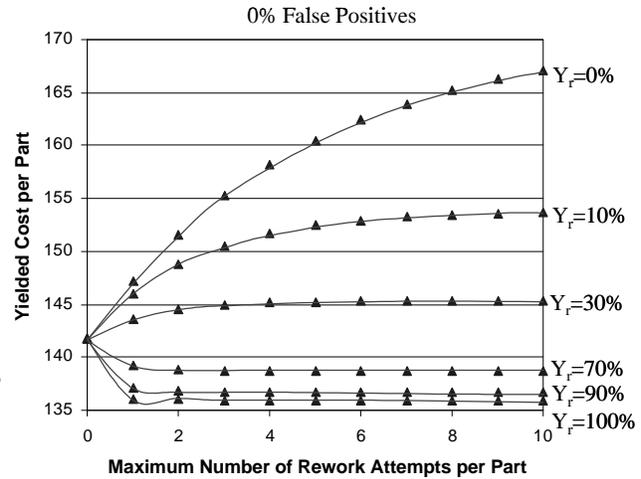
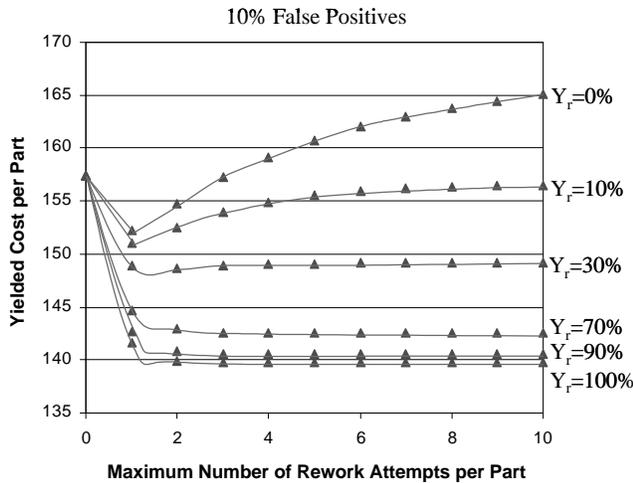


Figure 5 – Variation of final yielded cost (cost divided by yield) of parts that pass the test/diagnosis/rework process with the number of allowed rework attempts per part. In this example, false positives are only created on good parts.

Table II – Baseline data for example results.

C_{in}	100	f_c	70%	Y_{in}	90%
C_{test}	20	f_r	81%	$Y_{beforetest}$	97%
C_{diag}	10	f_d	100%	$Y_{aftertest}$	97%
C_{rew}	25	f_p	10%	Y_{rew}	90%
Rework attempts	2	False positives are created on good parts only			

Figure 5 shows that when false positives are created and rework yield is low, there is an optimum number of rework attempts per part (2 for $Y_{rew} = 30\%$, 1 for $Y_{rew} = 10\%$ or less). If no false positives are created, depending on the rework yield, the cost of performing the rework, and the rework success rate, rework may not be economically viable.

Figure 6 shows the effect of whether the false positives are created on just the good parts or all the parts. With no rework (in the zero rework attempts case, parts that are identified as defective are scrapped without diagnosis), if a fixed false positive fraction only affects good parts, the resulting per part yielded cost is higher than if the false positives affect all parts – while the same number of parts are scrapped in both cases, when the false positive fraction affects all parts, some defective parts are removed resulting in a low yielded cost. When many rework attempts are allowed, false positive creation on just good parts results in an overall lower yield part (because the false positive creation didn't remove any defective parts),

and also a lower overall cost part (because fewer parts were reworked) – the net effect in this case is that the overall yielded cost per part is lower.

Figure 7 shows an example from the Monte Carlo analysis. The solid line on the plot represents the

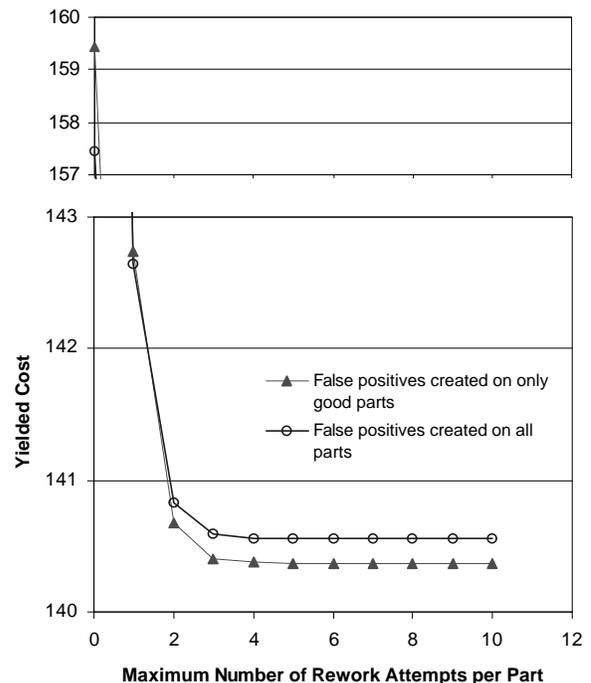


Figure 6 – Effect of the false positives definition on the part population.

solution found using only the most likely values of the input parameters. The two solutions with error bars have the same most likely values but a mixture of more realistic symmetric and asymmetric triangular distributions applied, Table III. The error bars represent plus or minus one standard deviation. The standard deviation of the solid squares is larger because the range of C_{test} values assumed in the distribution is larger. The standard deviations on the yielded cost are also found to be larger for smaller values of fault coverage using the data in Table III. This is due to an increase in the standard deviation of the yield as fault coverage drops (yield depends on quantities raised to the $1-f_c$ power).

Table III – Data for example Monte Carlo results. All distributions are triangular with the parameters denoted in the table by - most likely (low,high).

C_{in}	100 no distribution
C_{test}	20 (10,22)
C_{diag}	10 (5,15)
C_{rew}	25 (20,35)
Rework attempts	2
f_c	70% no distribution
f_r	81% (78,90)
f_d	100% (92,100)
f_p	10% (5,15)
Y_{in}	90% no distribution
$Y_{beforetest}$	97% (90,100)
$Y_{aftertest}$	97% (90,100)
Y_{rew}	90% (80,100)
False positives are created on good parts only	

4.2 Application of the Model to an AEPS Module

The model developed in this paper has been used to optimize the location of test/diagnosis/rework operations in the manufacturing process for an Advanced Electronic Power Systems (AEPS) module. AEPS refers to a system built around a packaging concept that replaces complex power electronics circuits with a single multi-function device that is intelligent and/or programmable. For example, depending on the application, an AEPS might be configured to act as an AC to DC rectifier, DC to AC inverter, motor controller, actuator, frequency changer, circuit breaker etc. The AEPS module considered here consists of 16 ThinPak™ devices [15], Figure 8. A ThinPak™ is a ceramic chip scale package for discrete

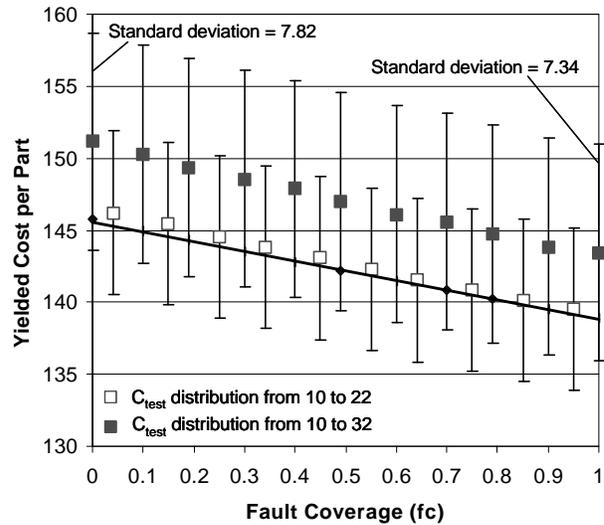


Figure 7 – Point solution versus solutions with distributed input parameters

3-terminal high power devices. A simplified process flow for the AEPS module is shown in Figure 9.⁴ The test economics challenge with the AEPS module is to determine where to perform test and rework operations: die level, device level, and/or module level.

Not all permutations of test and rework shown in Figure 9 were analyzed. Die level rework was omitted, the die used in the ThinPak™ devices are

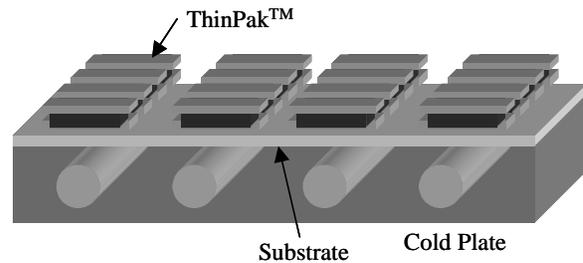


Figure 8 – AEPS module (600V half bridge) with 16 ThinPak™ devices mounted on it.

⁴ The multiplier step, denoted by “M”, appears twice in the AEPS module process flow. The “M=2” process step denotes the assembly of two copper straps with the die-alumina lid assembly to complete the Thinpak™ device level assembly. Similarly, the “M=16” process step denotes the assembly of sixteen Thinpak™ devices on the substrate during the module level assembly.

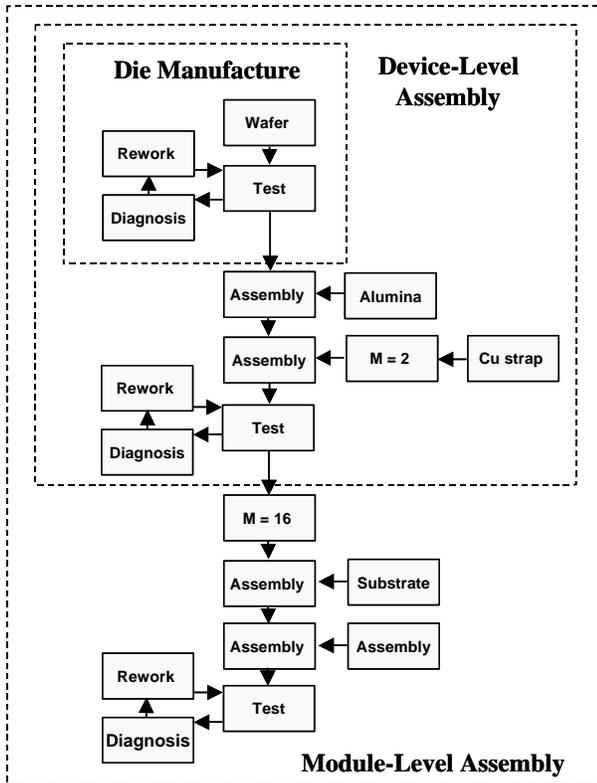


Figure 9 – Simplified process flow for the AEPS module including candidate test/diagnosis/rework operations.

relatively inexpensive and no practical methods of reworking defective die are available. We also did not consider device-level test or rework in the present analysis.

The analysis performed on the AEPS module includes a variable rework model where C_{rew} and Y_{rew} are not treated as constants (as in the analysis in Section 4.1), but are variables based on the assumption that rework is dominated by the replacement of defective ThinPak™ devices. C_{rew} and Y_{rew} are determined using,

$$C_{rew} = C_{rew-fixed} + C_{device} N_{device_i} (1 - Y_{device}) \quad (21)$$

$$Y_{rew} = Y_{rework\ process} Y_{device}^{N_{device_i} (1 - Y_{device})}, \quad (22)$$

where C_{device} and Y_{device} are the cost and yield of the ThinPak™ devices when they enter the module assembly process. N_{device_i} is the total number of ThinPak™ devices replaced in the previous rework attempt given by,

$$N_{device_i} = N_{device_{i-1}} (1 - Y_{device}) \quad (22)$$

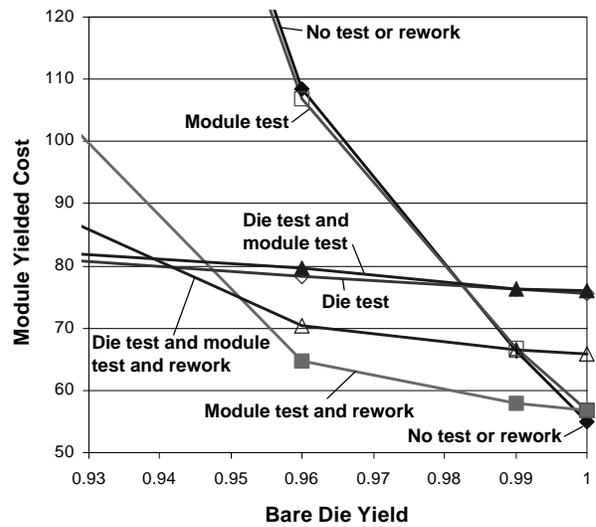


Figure 10 – Test/diagnosis/rework placement for an AEPS module containing 16 devices. The system yielded cost are means from Monte Carlo analysis.

where $N_{device_0} = 16$ in our example case.

Figure 10 shows results of an analysis on the AEPS module. When the yield of the die is 100%, no test or rework is the most economical solution (this result is intuitive). Module test is relatively inexpensive and scraps defective modules prior to shipping, however, it has overall effect on the yielded cost (the ratio of cost to yield). When die test is introduced, the cost shifts up by an amount equal to the test cost per die multiplied by 16. Again, performing module test along with die test improves the yield of modules exiting the process, but has little effect on the overall yielded cost. When module-level rework is performed, some of the scrapped modules are recovered thus reducing the cost. For die with yields between 0.998 and 0.952 module test and rework is the most economical. For $0.952 > yield > 0.942$ die test and module test and rework is best and for yield < 0.942 die test only is the best solution.

5. Discussion and Summary

This paper details a test/diagnosis/rework analysis model for use in technical cost modeling of electronic assemblies. The approach includes a model of test operations characterized by fault coverage, false positives, and defects introduced in test, in addition to rework and diagnosis operations that have variable success rates and their own defect introduction mechanisms. The model can accommodate an

arbitrary number of rework attempts on any given assembly and can be used to optimize the fault coverage and rework investment during system tradeoff analyses.

The method presented in this paper is appropriate for use when the entire test/diagnosis/rework is either

a) summarized into a single process where the describing parameters (e.g., f_c , f_p , C_{test} , C_{diag} , C_{rew} , ...) represent effective values averaged over a range of fault types. In this case the false positive fraction, f_p , should act only on good parts, i.e., parts without the fault(s) that the particular test step corresponds to.

b) divided into individual fault-specific processes, where the describing parameters represent values specific to a particular fault (in this case, Y_{in} would be with respect to a particular fault type). In this case the false positive fraction, f_p , should act on all parts.

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