Application-Specific Economic Analysis of Integral Passives in Printed Circuit Boards*

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***Abstract* - This paper summarizes an application-specific economic analysis of the conversion of discrete passive resistors and capacitors to integral passives that are embedded within a printed circuit board. In this study we assume that integral resistors are printed or plated directly onto wiring layers (as opposed to requiring a dedicated layer), that bypass capacitors are embedded by dielectric substitution into existing reference plane layers, and that singulated non-bypass capacitors are embedded using dedicated layer pair addition. The model presented performs three basic analyses: 1) Board size analysis is used to determine board sizes, layer counts, and the number of boards that can be fabricated on a panel; 2) Panel fabrication cost modeling including a cost of ownership model is used to determine the impact of throughput changes associated with fabricating integral passive panels; and 3) Assembly modeling is used to determine the cost of assembling all discrete components, and their associated inspection and rework. The combination of these three analyses is used to evaluate size/cost tradeoffs for an example board.**

I. INTRODUCTION

The use of discrete passive components in electronic systems has continued to increase even as the degree of system integration has increased. To meet the increased demand for passive devices some passive devices are fabricated within ICs, however, designing passives into ICs limits the IC's flexibility for many uses. In addition, real estate on an IC is usually more expensive than real estate on a board.

The trend above not only requires more passives to be purchased and assembled to the system, but also suggests that discrete passives will consume increasing amounts of board area and assembly time. The electronics assembly industry has responded to the challenge by developing higher-speed chip shooters (>100,000 placements per hour are possible), and the passive components industry has responded by producing smaller passive components.

An alternative solution to the passive growth trend is integrating multiple passives together within a single package (networks or arrays of passives). This approach can reduce assembly costs, however, the unit cost of integrated passives remains high (higher than the discrete passive components they replace). Even with the use of small dimension passives and judicious insertion of network or array passive components, many applications still cannot meet performance and size requirements. Integral passives (IPs) were introduced to address these needs. IPs are fabricated within substrates, and while IPs will never replace all passive components, they provide a potential advantage for many applications including:

- Increased circuit density
- Decreased product weight
- Improved electrical properties
- Cost reduction
- Increased product quality
- Improved reliability.

Potentially the biggest single question about integral passives is their cost, "…of all the inhibitors to achieving an acceptable market for integral substrates, the demonstration of cost savings is paramount" [1]. There is considerable controversy in technology circles as to whether applications fabricated using integral passives will be able to compete economically with discrete passive technology. On the bright side, the use of integral passives reduces assembly costs, shrinks the required board size, and negates the cost of purchasing and handling discrete passive components. However, these economic advantages must be traded off against the increased cost (per unit area) of boards fabricated with integral passives (a situation that will not disappear over time) and decreased throughput of the board fabrication process.

II. MODEL DEVELOPMENT

The objective of the model demonstrated in this paper is to capture the economic impact of the following competing effects when integrated components are present in the board:

* This work was supported in part by the Advanced Embedded Passives Technology (AEPT) Consortium under the U.S. Department of Commerce, National Institute for Standards and Technology, Advanced Technology Program, Cooperative Agreement Number 70NANB8H4025.

- Decreased board area due to a reduction in the number of discrete passive components
- Decreased wiring density requirements due to the integration of passives
- Increased wiring density requirements due to the decreased size of the board
- Increased number of boards fabricated on a panel due to decreased board size
- Increased board cost per unit area
- Decreased board yield
- Decreased board fabrication throughput
- Decreased assembly costs
- Increased overall assembly yield
- Decreased assembly-level rework.

Due to the opposing nature of many of the effects listed above, the overall economic impact of replacing discrete passives with integral passives is not trivial to determine and, in general, yields application-specific guidelines instead of general rules of thumb. In fact the very nature of tradeoff analysis is one in which *the greater the detail necessary to accurately model a system, the less general and more application-specific the result*.

Several authors, [1]-[7], have addressed cost analysis for integral passives and thus provide varying degrees of insight into the economic impact of converting discrete passives to embedded. The target of all these economic analyses is to determine the effective cost of converting selected discrete passive components to integral components. The most common approach to economic analysis of integral passives is to: 1) reduce the system cost by the purchase price and conversion costs (handling, storage and assembly) associated with the replaced discrete passives, 2) reduce the board size by the sum of the layout areas associated with the replaced discrete passives and determine the new number of boards on the panel, and 3) determine the new board cost based on a higher per unit area cost for the integral passive panel fabrication and the new number-up computed in step 2. The results of these three steps determines the new system cost. The effects included in this first-order approach are critical, however, the approach generally ignores several additional elements, most notably: decreased throughput for integral passive board fabrication means that board fabricators will have to charge higher profit margins on integral passive boards to justify their production on lines that could otherwise be producing conventional boards; routing analysis of the board to determine not only what layers may be omitted, but what layers may have to be added to maintain sufficient wiring capacity as passives are integrated and the board is allowed to shrink; yield of both discrete passive components and the variation in board yield due to the integration of passives; and potential reductions in rework costs (due to both assembly defects and intrinsic functional defects) associated with discrete passives.

In the model used here, we incorporate quantitative routing estimation and assess board fabrication throughput impacts for setting profit margins on board fabrication, effects that have not been included previously. We also make the following technology assumptions:

1) Integral resistors are fabricated directly on wiring layers via printing or plating (e.g., [8], [9]) – as opposed to requiring dedicated integral resistor layers as assumed previously, [4] and [5].
2) Bypass capacitors are embedded by dielectric substitution into an existing reference plane layer (as opposed to layer pair addition).
3) Singulated integral capacitors are fabricated via dedicated layer pair addition.

The model used for analyzing integral passive cost tradeoffs is summarized in Figure 1. Detailed formulations are included in [10].

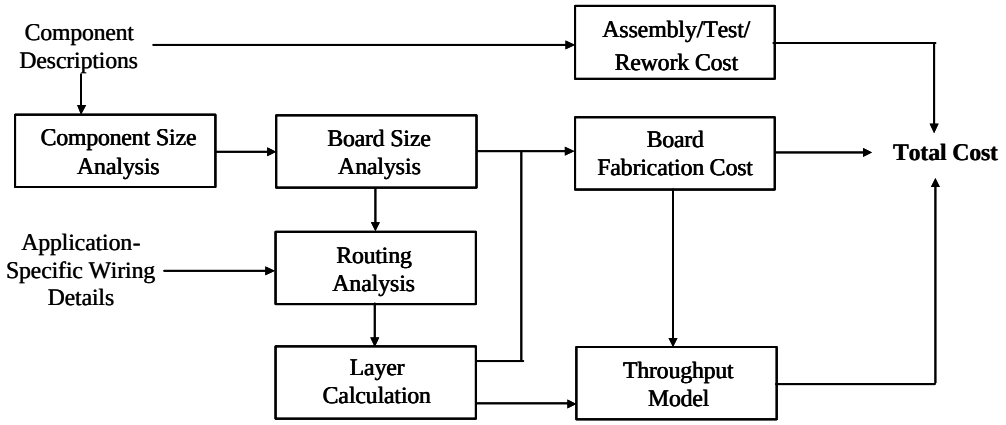

Figure 1 – Summary of cost model developed for the analysis of integral passive cost impacts on electronic systems, [10].

III. Throughput Analysis

A fundamental issue not addressed in previous cost analyses associated with integral passives is the throughput of the process that is used to manufacture the boards. Throughput is a measure of the number of products that can be produced in a given period of time, and is the inverse of cycle time (the time elapsed between completed products). Throughput is key to understanding the profit margin that will be required to justify manufacturing integral passive boards.

The situation faced by the board manufacturer is the following: assume that there are two types of boards that could be fabricated on a process line, one is a conventional board with a known profit margin and the other is an integral passive board. To simplify the problem, assume that the number of boards to be manufactured will be the same for both types of board. The cycle time of the integral passive process will be longer than that for conventional boards. The manufacturing cost of the integral passive board is larger. The manufacturer must decide what profit margin to use for the integral passive board so that the total profit per unit time made by selling integral passive boards equals or exceeds what can be made by selling the conventional boards. This is necessary to justify the use of a line to fabricate integral passive boards when it would otherwise be producing conventional boards.

To explore throughput effects and determine the relative profit margins of the printed circuit boards, a cost of ownership (COO) model has been developed. The COO model captures the costs due to maintenance (scheduled and unscheduled), yield loss, cycle time variations, and change overs.

Example results generated using the model are shown in Figure 2. If cycle times of layer pair production for conventional and integral passive layers, and the average profit margin for conventional boards are known, the minimum required profit margin for integral passive board fabrication can be determined. The cost of ownership model must be repeated for each board manufacturing scenario since the number of layers in the multilayer board and the dimensions of the individual board are application-specific.

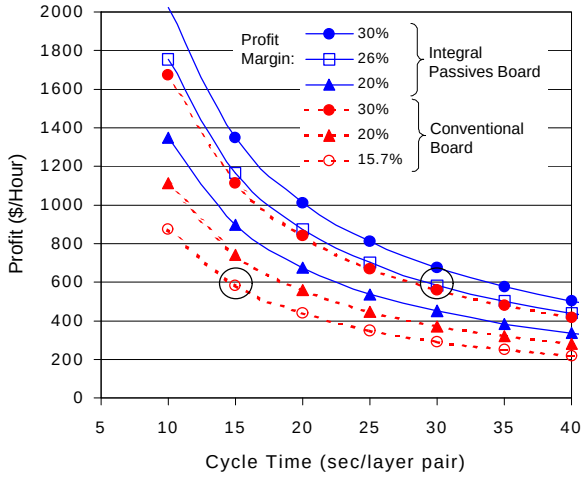

Figure 2 - The relationship between profit margin and production cycle time for conventional and integral passive board fabrication.

The example shown in Figure 2 indicates that if, conventional boards have a 15.7% profit margin and 15 second cycle time (per layer pair), then 30 second per layer pair integral passive board production is only feasible for profit margins of 26% or more. The most important property from this analysis is the difference between the profit margins, the tradeoff analysis results are much less dependent on the absolute values of the profit margins. We consistently observe profit margin differences of ~10%. The analysis presented in Section IV assumes profit margins that make the average profit per hour of each type of board fabrication equal.

IV. Analysis Results

In this section we present the results of size/cost tradeoff analyses performed on a picocell board. It is not the intent of this analysis to prove that integral passives lead to less expensive systems, rather we wish to understand the economic realities should we decide to use integral passives.

The relevant characteristics of the picocell application are given in Table I.

Table I
Picocell Board Characteristics

Number of Embeddable Discrete Resistors	27 (< 100 Ω) 19 (100-1000 Ω) 22 (1 – 10 kΩ) 1 (10 – 100 kΩ) 1 (>100 kΩ)
Size of Embeddable Discrete Resistors	69 0805 (80x50 mils) 1 1201 (120x100 mils)
Number of Embeddable Discrete Capacitors	1 (< 100 pF) 29 (100 – 1000 pF) 13 (1 – 10 nF)
Size of Embeddable Discrete Capacitors	43 0805 (80x50 mils)
Discrete Passive Cost	$0.0045 per part
Conversion Cost (excluding assembly)	$0.015 per part
Board Size	2.27 x 6.87 inches
Number of Board Layers	10

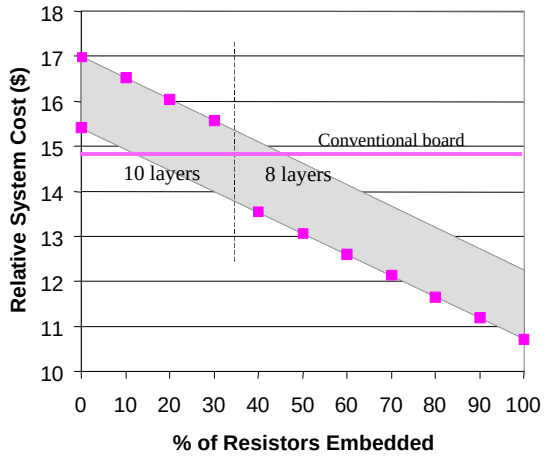

Figure 3. The economics of integral resistors for the picocell board application. The data points represent one integral passive solution for a specific routing resource assumption (assumption of the ratio of resources actually used to route the conventional implementation of the board and the theoretical maximum amount of resources that could be used), the band represents all possible integral passive solutions for this application; the solid horizontal line is the system cost of conventional implementations.

Figure 3 shows analysis results for the picocell board as discrete resistors are replaced by integral resistors (capacitors are not integrated in Figure 3). Relative system cost is plotted In Figure 3 and throughout this section indicating the system cost less the cost of all non-embeddable components and functional testing. The specific solution (data points) in Figure 3 indicates that the integral passive board becomes economical when approximately 35% of the embeddable discrete resistors are embedded[1]. The data point at $15.40 when no resistors are embedded represents the board price increase due only to the need for a higher profit margin to justify integral passive board fabrication (see Section III). The next point on the vertical axis ($17) is the relative cost of the system when the first resistor is embedded.

A discontinuity in the specific integral passive board data is labeled on the plot. In this case, embedding of discrete resistors simplifies the routing problem enough (omission of vias and capture pads) to allow the removal of a layer pair causing the drop in cost. However, in the picocell board case, the board size never decreases sufficiently to allow more boards to be fabricated on an 18 x 24 inch panel, however,

[1] The integral resistors considered in this study are considerably more economical than integral resistors in previous studies due to the assumption of fabrication of the integral resistors directly on wiring layers as opposed to dedicated integral resistor layer.

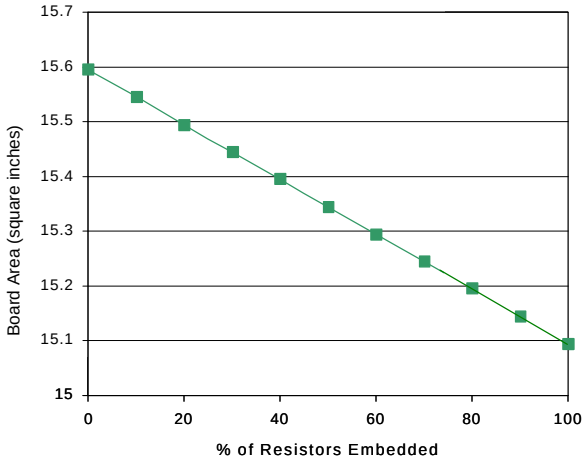

Figure 4. Board size decrease with resistor embedding for picocell board application.

potential board size decreases are still important to the customer. Figure 4 shows the board area change as fraction of integral resistors is varied.

Next consider the integration of capacitors. Figure 5 shows the relative system costs as the embeddable capacitors are integrated (none of the embeddable discrete resistors are embedded in Figure 5). Since embedding of bypass capacitors requires material replacement and non-bypass capacitors requires the addition of an extra layer pair (for the technology we assumed), the very first bypass or non-bypass capacitor embedded increases the cost of the board dramatically, but as more capacitors are embedded, the added cost of the replacement material and/or additional layer is gradually offset by the avoidance of discrete capacitor part and assembly costs. The driver that determines

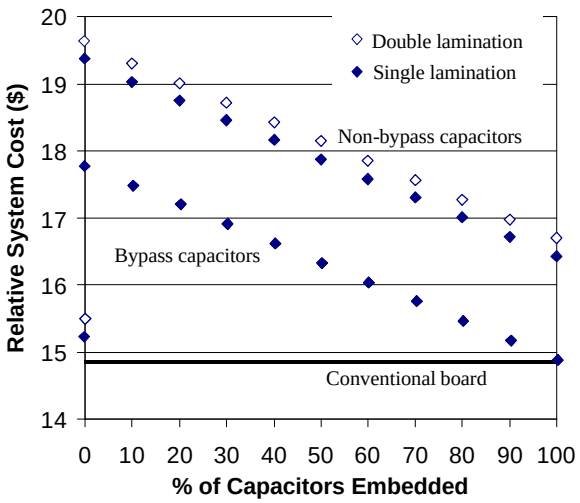

Figure 5. Capacitor embedding for the picocell board application.

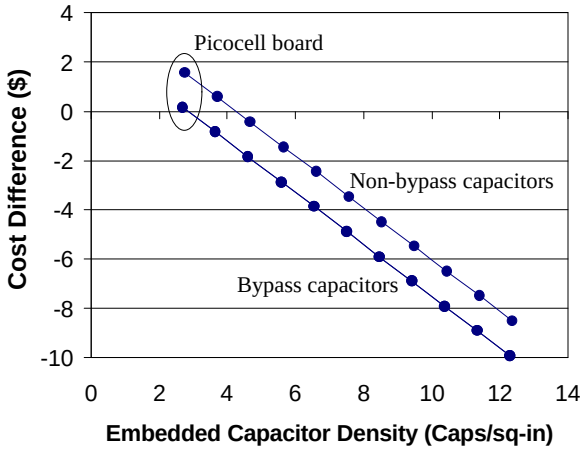

Figure 6. The impact of embeddable capacitor density on system cost for the picocell board application.

whether capacitor embedding is economical or not, is the density of embeddable discrete capacitors on the board. Figure 6 shows that when additional embeddable capacitors are added to the picocell board application (thus increasing the capacitor density), non-bypass integral capacitors would become economically viable at approximately 4.4 capacitors/square inch, whereas the actual picocell board application has only 2.76 capacitors/square inch; bypass integral capacitors become economical at 2.9 capacitors/square inch.

V. Discussion and Conclusions

In this paper we have presented the results of an application-specific economic analysis of the conversion of discrete passive components (resistors and capacitors) to integral passives that are embedded within a printed circuit board. The model has been demonstrated on a picocell board. In this case and others not included here, we found integral resistors to be generally cost effective with the most significant economic impact resulting from either number-up increases due to board size reductions, or layer count decreases due to reductions in routing requirements. Note, we considered integral resistors fabricated directly on wiring layers (as opposed to dedicated integral resistor layers assumed in previous studies [4] and [5]) therefore, we can not generalize to components per unit area because it is board fabrication profit margin driven, which is a fractional increase in board cost and much smaller in absolute terms for high number-up, whereas cost reduction is through omission of discrete part costs. As expected, when a technology that adds resistors directly to the wiring layers is used, integral resistors become economically viable when considerably fewer are integrated than for layer addition technologies.

For the applications considered, integral bypass capacitors become economical when the capacitor density (number of discrete capacitors per square inch) reaches 2.9 – 3.1 capacitors/square inch or greater, integral non-bypass capacitors become economical when the capacitor density reaches 4.4 – 4.6 capacitors/square inch or greater, which is considerably smaller than the 3 components per square cm previously proposed [11]. This is due to the material costs assumed (from the NEMI roadmap, [12]), which represent mature technology material costs.

It must be reiterated that due to the opposing nature of many of the effects listed outlined in this paper, the overall economic impact of replacing discrete passives with integral passives, in general, yields application-specific guidelines instead of general rules of thumb. We also need to point out several factors that should be kept in mind when interpreting the results in this paper:

1) Several system implementation details are not addressed in this analysis including:
   i. Waste disposition in board fabrication – we only account for additional waste disposition costs associated with the fabrication of integral passive boards in the profit margin differential.
   ii. Non-homogeneous panelization – some panel fabrication technologies and materials allow boards to be laid out on the panel with 90 degree relative rotations resulting in the potential for more boards on a panel, we have assumed homogeneous panelization in this analysis.
   iii. We have not considered the possibility raised in [1] that the conversion of discrete to integral passives may allow some double-sided assemblies to become single sided thus saving significant assembly costs.
2) With any tradeoff analysis, the results are only as good as the input data, i.e., inaccuracies in the input data will change the results of the analysis.
3) In addition to the direct effects on system cost discussed in this paper, there are many other "life cycle" effects on the system cost. These effects include the changes in the system reliability, performance, end-of-life options and the design overhead that constitute effective life cycle costs. For some systems, integral passives may also affect the upgradability and field repairability of the system.

ACKNOWLEDGMENT

The authors wish to acknowledge the members of the Advanced Embedded Passives Technology (AEPT) Consortium – NCMS, ITRI, 3M, Compaq Computer, Delphi Delco Electronics, DuPont Photopolymer & Electronic Materials, DuPont High Performance Films, ESI, Foresight Systems, MacDermid, Merix Corporation, MicroFab, Nortel Networks, ORMET Corporation, and Sanmina; and the members of the NEMI Passive Components Technology Working Group for their inputs and comments on this work.

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