

Using Embedded Resistor Emulation and Trimming to Demonstrate Measurement Methods and Associated Engineering Model Development*

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Embedded resistors are planar resistors that are fabricated inside printed circuit boards and used as an alternative to discrete resistor components that are mounted on the surface of the boards. The successful use of embedded resistors in many applications requires that the resistors be trimmed to required design values prior to lamination into printed circuit boards. This paper describes a simple emulation approach utilizing conductive paper that can be used to characterize embedded resistor operation and experimentally optimize resistor trimming patterns. We also describe a hierarchy of simple modeling approaches appropriate to both college engineering students and pre-college students that can be verified with the experimental results, and used to extend the experimental trimming analysis. The methodology described in this paper is a simple and effective approach for demonstrating a combination of measurement methods, uncertainty analysis, and associated engineering model development.

Keywords: embedded resistors; embedded passives; trimming

INTRODUCTION

EMBEDDING PASSIVE components (capacitors, resistors, and possibly inductors) within printed circuit boards is one of a series of technology advances enabling performance increases, size and weight reductions, and potentially cost advantages in the manufacturing of electronic systems [1]. Figure 1 shows a comparison of surface mount and embedded resistors.

Multilayer printed circuit boards are fabricated starting with dielectric layers that are plated on both sides with copper. Application-specific conductor patterns are created on each side of the dielectric using a photosensitive resist and etching to remove the unnecessary copper. These patterned 'layer pairs' are stacked with a B-stage epoxy between them and laminated using high temperature and pressure. Holes can be drilled and plated in the laminated stack to create vertical connections. [Note, there are many printed circuit board fabrication process and material variations, e.g., [2]. The process described here is one simplified approach.] Embedded resistors (also called integral resistors) are fabricated by plating or printing a resistive material onto a layer that will be part of a printed circuit board (additive process), or alternatively, using a subtractive

process that starts with a layer pair that is pre-coated with resistive material that is selectively removed to create the resistors. The layer containing the resistor is laminated together with other layers to make the finished printed circuit board.

One significant factor governing the applicability of embedded resistors is their tolerance level. The tolerance to which a resistor can be fabricated determines the applications for which it can be used and potentially affects its impact on the yield of the product. While discrete surface mount resistors can be pre-sorted by value, or even replaced during assembly when their value is not within the required range, embedded resistors provide no such opportunity and must be within design tolerance value before the board fabrication process is completed. Therefore, embedded resistors, depending on their method of fabrication and the application for which they are used, may be 'trimmed' to the desired value after they are fabricated. To allow for trimming, embedded resistors are designed to have a resistance value that is lower than that needed by the application. Trimming is then accomplished by cutting holes into the resistor in order to increase its resistance value.

Embedded resistors are normally trimmed using a laser to micromachine a trough in the resistive element, [3]. The length and path-shape of the trough determine the characteristics of the resistance change obtained. Several different path-shapes can be used depending on the specific

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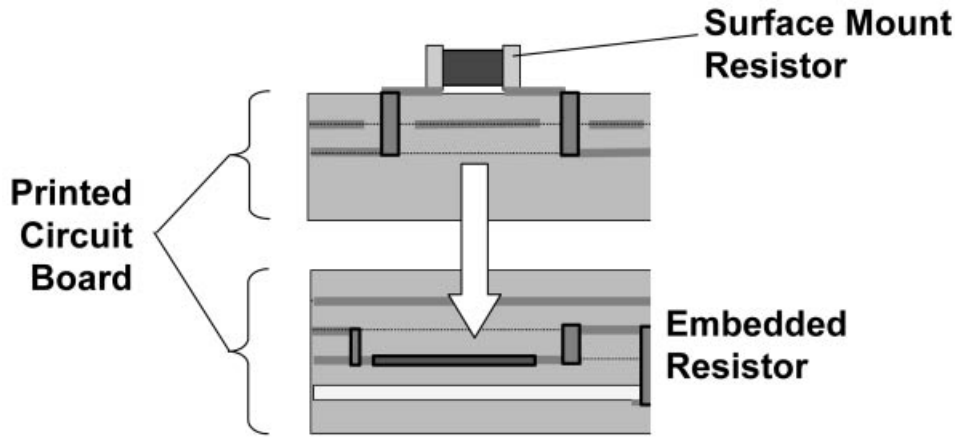


Fig. 1. Surface mount and embedded resistors.

trimming requirements. As the laser cuts the trough, the resistor value is measured and used as feedback to control the trimming process. Unfortunately, laser trimming equipment is expensive and the process of trimming potentially represents a throughput bottleneck in the board fabrication process. Trimming has been identified as one possible impediment to the widespread use of embedded resistors [4, 5].

This paper describes a simple methodology for experimentally assessing embedded resistor trim patterns that can be supplemented with the development and verification of simple models that can be used to extend the experimental results. The work described herein has been successfully used by both pre-college high school students and within an undergraduate electronic packaging curriculum for college-level mechanical and electrical engineering students. Students are motivated by being able to work on a topic that is at the forefront of electronic systems design and fabrication, yet conceptually simple enough so as not to defeat their limited knowledge of physics and engineering. The experiment and modeling described in the paper provides students with an understanding of resistance, resistance measurements, experimental uncertainty analysis, the engineering model development and verification process, and the use of models to extend experimental results.

EMULATING EMBEDDED RESISTORS

For a constant sheet resistance (ohms per square), the resistance of a planar resistor does not change with size (i.e., length or width) as long as the ratio of length to width ('aspect ratio') is constant,

$$R = \frac{\rho L}{A} = \frac{\rho L}{TW} = \frac{\rho}{T} \left(\frac{L}{W} \right) = R \left(\frac{L}{W} \right), \quad (1)$$

where ρ is the bulk resistivity, A is the cross-sectional area of the resistor, R is the 'sheet

resistance' (in ohms per square), and L , W , and T are the length, width, and thickness of the resistor. Therefore, for a constant aspect ratio (L/W), a small planar resistor (dimensions in the thousands of the inch) has the same resistance characteristics as a large area planar resistor (dimensions of inches), and trimming of small resistors can be emulated using large area resistors.

To emulate planar embedded resistors, we used conductive paper purchased from PASCO Scientific (Model PK-9025). This type of paper is usually used for tracing lines of equipotential and electric fields, and comes in 8.5×11 inch pages with a centimeter grid printed on it. Prior to exploring trimming of the resistors, each page of paper is cut to the desired resistor shape—in our case approximately 1 cm was removed from all the edges of the pages and the remaining page is cut in half to create two 28×10 cm resistors. In order to measure the resistance, metal clamps are placed on the ends of the resistor and an ohmmeter is attached to the clamps via alligator clips, Fig. 2. Students make an initial set of measurements on a single piece of paper by assembling the test setup, measuring, and disassembling the test setup, then repeating the process 10–15 times. The first thing noticed is that the resistance of the conductive paper varies from page-to-page. In order to make the measurements from different pages comparable, a page-specific 'normalization' must be determined. In order to normalize a page's mean resistance to $65 \text{ k}\Omega$, $65 \text{ k}\Omega$ was divided by the mean resistance from the initial measurements for the page to obtain a scaling factor, then each measurement from that page of paper (as it is trimmed) is first multiplied by the scaling factor before comparison with other pages. [For the 28×10 cm resistors suggested, $65 \text{ k}\Omega$ was found to be the approximate average resistance value over many pages of conductive paper and was therefore used as the normalization target.]

The way that the page measurements are normalized adjusts for page-to-page variation in resistance due to variations in the sheet resistance (R) but does not affect variations in the contact to

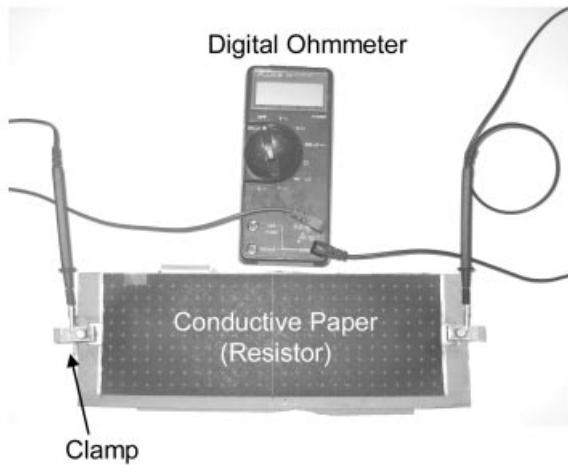


Fig. 2. Experimental setup.

the conductive paper or other series resistance effect within the measurement path. Variations in the sheet resistance could be due to thickness variations in the conductive coating or moisture absorption by the paper. Variations in the measurement path are quantified as measurement uncertainties.

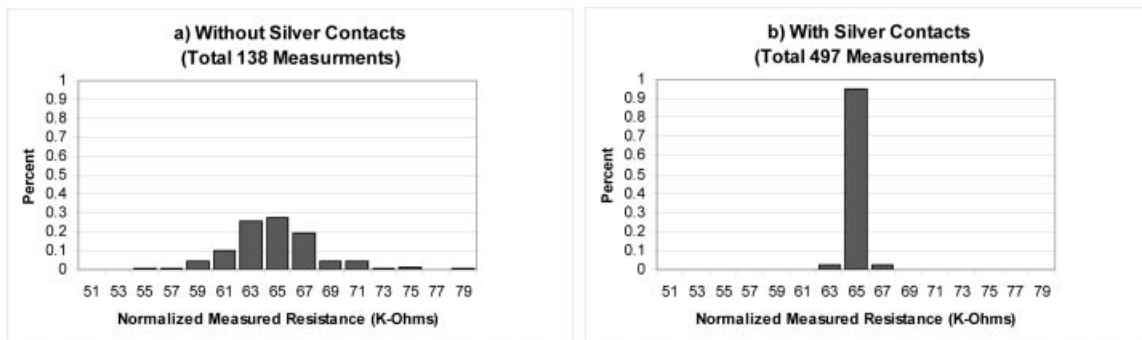
Figure 3(a) shows the distribution of normalized measured resistance when the clamps are attached directly to the conductive paper. Students discover that when contacts are added to the ends of the conductive paper using a thin strip (approximately 0.3 cm wide) of conductive silver paint, the measurement error can be reduced from a 6.6% (4.3 k Ω) standard deviation to 0.9% (0.59 k Ω) standard deviation (Fig. 3(b)). The silver contacts make the measurement less sensitive to where the clamp was placed, and the pressure with which the clamp is applied.

Several physical effects on the resistance measurement can also be explored including the temperature coefficient of resistance (TCR). The TCR can be found by measuring the resistance of the paper at different temperatures. The slope of the temperature versus resistance relation allows students to draw conclusions about the type of material used to coat the conductive paper (e.g., a negative slope indicates that the material is a

semiconductor). Students can also check to see if thermocouple effects are significant by switching the ohmmeter connection and determining if there is any significant change in the resistance measured. In our experience, thermocouple effects, if present, are smaller than the measurement uncertainty. [The thermocouple effect is due to the thermal emf generated by the change in the temperature at the junction of the conductive paper and the silver contacts on each end, which form thermocouples. If the temperature at both ends of the resistor is the same, the thermal emfs will cancel and the resistance measured is the same, regardless of the way the meter is connected. If the temperature at one end is different from the other than the measured resistance will differ when the meter connections are switched.]

RESISTOR TRIMMING: EXPERIMENTAL RESULTS

Once the baseline measurements are made on a page of paper and the page-specific normalization determined, the pages are ready for trimming. Several different types of trimming patterns can be explored, Fig. 4. The trim patterns are created using scissors or a razor blade to cut one square centimeter from the paper at a time and measuring the resulting resistance. By varying the length and location of the trim, the example results shown in Fig. 5 can be obtained. The plots show the progression that the resistance makes as the length of the trim increases. Figure 5(a) shows the trimming results for a Single-Dive trim pattern. The results indicate that, regardless of location, the resistance is the same for all cases until the trim length exceeds four centimeters. However, if the length of the trim exceeds four centimeters, then a trim near the edge will result in more resistance increase. Figure 5(b) shows the trimming results for an L-Cut. For the example shown in Fig. 5(b), resistors were trimmed so that the trim changed direction after three or six centimeters. The change of direction can be seen on this graph when the slope of the line changes. Figure 5(c) shows a

Fig. 3. Distribution of normalized resistance measurements with and without conductive silver contacts. The mean of both distributions is 65 k Ω .

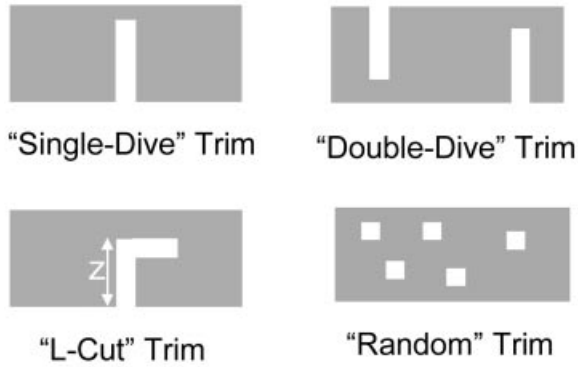


Fig. 4. Example trimming patterns that can be considered.

comparison of trimming results of several trimming patterns—the single-dive, the double-dive, the L-Cut, and a random trim. The patterns varied in shape as well as location, and the results are illustrated in the graph.

RESISTOR TRIMMING: MODELING

One advantage of using embedded resistor trimming as an engineering educational tool is that a hierarchy of simple models can be developed that readily match actual experimental trimming results. The modeling methodology presented in this paper has been used for both pre-college (pre-calculus) students and college engineering students making use of their respective mathematical education levels.

Simple pre-calculus models

Students can construct a hierarchy of simple models based on summing resistors in series. An evolution of models used to model the single-dive trim is shown in Fig. 6. The shape of each series resistor is determined by assuming the current path. Variables in the models are the lengths and widths of the resistor, the location and length of the trim, and the number of rectangles used in the model. For example, the formulations for a single-dive are given by,

$$R = R_1 + R_2 + R_3, \quad (2)$$

which becomes

Model 1:

$$R = R\left(\frac{x_1}{W}\right) + R\left(\frac{x_2}{W-D}\right) + R\left(\frac{x_3}{W}\right) \quad (3a)$$

Model 2:

$$R = R \sum_{i=1}^n \left[\frac{\frac{x_1}{n}}{W - \left(\frac{D}{n}\right)\left(\frac{2i-1}{2}\right)} \right] + R\left(\frac{x_2}{W-D}\right) + R \sum_{i=1}^m \left[\frac{\frac{x_3}{m}}{W - \left(\frac{D}{m}\right)\left(\frac{2i-1}{2}\right)} \right], \quad (3b)$$

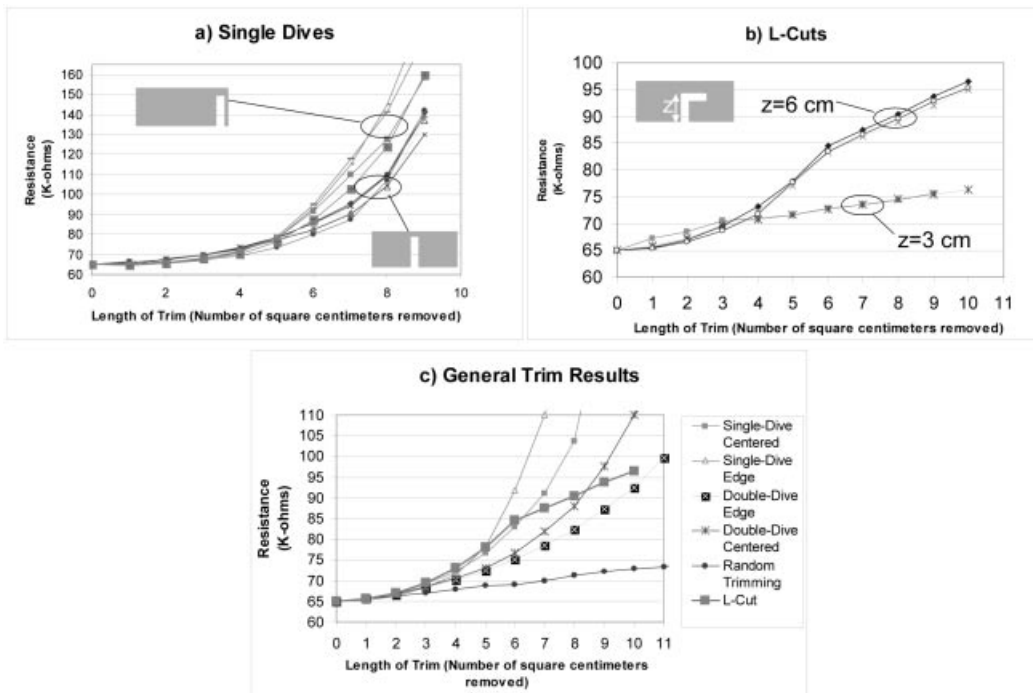


Fig. 5. Resistance as a function of the total trim length for (a) Single-Dives, (b) L-Cut and (c) a selection of different trimming types.

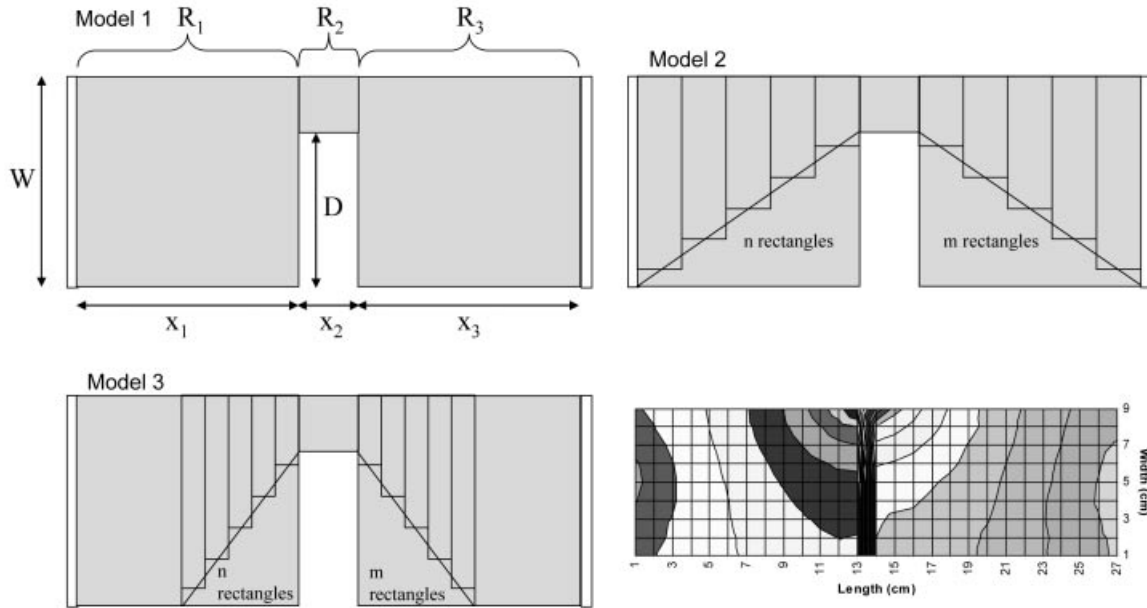


Fig. 6. Evolution of models. The bottom right shows a contour plot of equipotential lines in a Single-Dive trimmed resistor (only the potentials of points internal to the resistor are shown).

Model 3:

$$\begin{aligned}
 R = & R \frac{x_1}{2W} + R \sum_{i=1}^n \left[\frac{\frac{x_1}{2n}}{W - \left(\frac{D}{n}\right) \left(\frac{2i-i}{2}\right)} \right] \\
 & + R \left(\frac{x_2}{W-D} \right) \\
 & + R \sum_{i=1}^m \left[\frac{\frac{x_3}{2m}}{W - \left(\frac{D}{m}\right) \left(\frac{2i-1}{2}\right)} \right] + R \frac{x_3}{2W}
 \end{aligned} \quad (3c)$$

where n and m are the number of rectangles on either side of the trim, $R = 65/(28/10) = 23.21 \text{ k}\Omega$ and the other variables in (3) are defined in Fig. 6. Students formulate the models themselves and implement the models on a spreadsheet. Students

will find that Model 1 under predicts the resistance and that Model 2 over predicts the resistance, Fig. 7(a). To develop a better model, students can apply a current across a trimmed resistor and use the ohmmeter to probe the potential as a function of location within the trimmed resistor. By creating a contour plot showing lines of equipotential (Fig. 6) models similar to Model 3 can be inferred. [Equipotential lines connect a set of points for which the potential difference (or voltage) is a constant value. The potential difference can be determined by placing a voltage source across the resistor, connecting one end of a voltmeter to the grounded end and measuring the voltage at each point in the resistor (the PASCO paper has a 1 centimeter grid pre-printed on it that can be used to define measurement points). The direction of the electric field is always perpendicular to equipotential lines and its strength at various points in the resistor can be inferred from the distance between the equipotential lines.]

Model 3 assumes a uniform current flow across

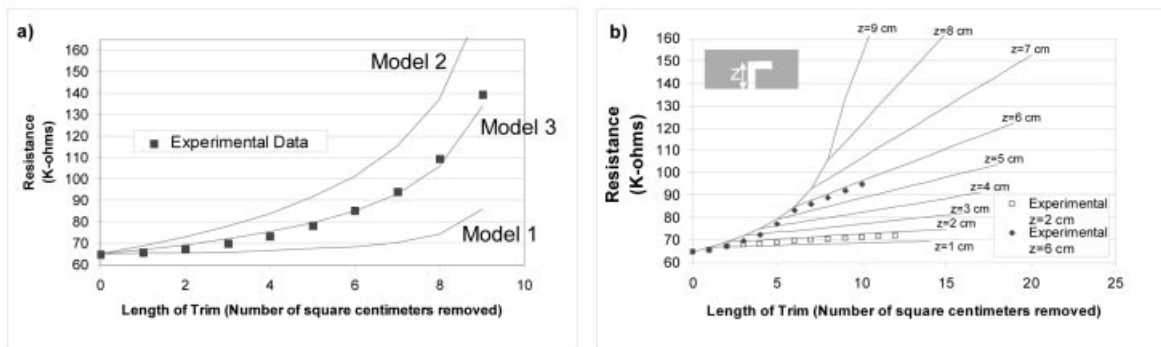


Fig. 7. Modeling results: (a) Model 1, 2, and 3 results compared with experimental measurements for a centered single-dive trim; (b) Model 3 results for L-cut trimming.

the resistor for the first half of the distance between the contact and the trim, then the effective cross-sectional area decreases linearly to the resistor's thinnest point. Figure 7(a) shows that Model 3 does a good job of fitting the single-dive trimming experimental results. In Fig. 7(b), Model 3 is applied to L-cut trims. Figure 7(b) shows a range of cases where the depth of the initial portion of the trim is varied. In this case, the model is used to extend the experimental results and produce a family of results for various values of z .

More advanced models

College-level engineering students who have a calculus background are expected to construct models that are more sophisticated. For example, the formulation corresponding to Model 2 is given by

$$\begin{aligned} R &= R_1 + R_2 + R_3 \\ &= R \int_0^{x_1} \frac{dx}{W - \frac{D}{x_1}x} + R \left(\frac{x_2}{W - D} \right) \\ &\quad + R \int_0^{x_3} \frac{dx}{W - \frac{D}{x_3}x}, \end{aligned} \quad (4)$$

which reduces to

$$R = R \left[\left(\frac{x_1 + x_3}{D} \right) \ln \left(\frac{W}{W - D} \right) + \left(\frac{x_2}{W - D} \right) \right]. \quad (5)$$

Students are expected to check their formulation by demonstrating that the model in (3b) limits to the model in (5) when n and m become large.

DISCUSSION

This paper describes an experiment coupled with model development that is attractive to students because of its simplicity, open-ended nature, and relevance to state-of-the-art electronic systems design and fabrication. Even given its simplicity, several findings clearly emerge.

1. Different trimming patterns result in varying rates of resistance increase and/or final resistance. For example, a 'single-dive' produces a high rate of resistance increase, i.e., the 'single-dive' trim pattern would be acceptable if reaching a target resistance was desired in a short amount of time. The 'double-dive' trim pattern shown in Fig. 4 (specific results for double-dive

trims are shown on Fig. 5(c)) yields a slightly lower rate of resistance increase. Both the single-dive and double-dive trims are ideal for quickly (with a minimum of trim length) approaching a high target resistance, i.e., one that is considerably higher than the initial resistance of the resistor. However, if there is a risk of trimming errors, i.e., trimming too much or too far, then the single- and double-dive trim patterns may not be preferred since the rate of change of the resistance near the end of the trim is large. Trimming errors can occur due to material inconsistencies, i.e., if a void in the embedded resistor material is encountered during the trimming process, the resistance value may 'jump' when the trimming trough reaches it. The risk of material inconsistencies depends on the particular process used to create the embedded resistor. [One method of reworking embedded resistors (that have been over trimmed) is to print conductive ink on the surface of the embedded resistor thus adding a lower value parallel resistor that effectively 'trims down' the resistor value, [6].]

2. The 'L-cut' trim pattern has different characteristics, in that the rate of increase changes when the trim changes direction. As the initial trim is made (perpendicular to the current flow in the resistor), the resistance steadily increases as it would for a single-dive trim, but when the trim changes direction to become parallel to the current flow, the rate of resistance increase slows (see Fig. 5(b)). The 'L-cut' trim pattern is ideal for balancing quick trimming with low risk.

Detailed numerical models of resistor trimming exist (e.g., [7–9]) but are generally too advanced for pre-college and undergraduate college students to obtain educational value from, therefore, simple models of the sort suggested herein are more reasonable for educational purposes. Students are able to use the simple models to confirm that the characteristics they are observing experimentally are in fact not artifacts of the measurement process, but actually the effects they are trying to measure. Many other trim variations and locations can be experimented with and the simple models suggested herein can be modified and applied to other trimming patterns.

Emulating embedded resistor trimming is an effective vehicle for introducing both pre-college and college students to simple measurements coupled with engineering modeling.

REFERENCES

1. R. K. Ulrich and L. W. Schaper, *Integrated Passive Component Technology*, John Wiley & Sons, Inc., (2003).
2. C.F. Coombs, *Printed Circuit Board Handbook*, 5th edition, McGraw-Hill, (2001).
3. K. Fjeldsted and S. L. Chase, Embedded passives: Laser trimmed resistors, *CircuitTree*, March 2002, pp. 70–76.

4. *Passive Components Technology Roadmap*, National Electronics Manufacturing Technology Roadmaps, NEMI, Inc. (2000).
5. P. Sandborn, An assessment of embedded resistor trimming and rework, *IEEE Trans. on Electronics Packaging Manufacturing*, **28**(2), 2005, pp. 176–186.
6. V. G. Shah and D. J. Hayes, Trimming and printing of embedded resistors using demand-mode ink-jet technology and conductor polymer, *Proceedings of the Technical Conference IPC Printed Circuits Expo*, March (2002), pp. S14-4-1 to S14-4-5.
7. B. Postlethwaite, CAD simulations improve resistor trimming results, *Hybrid Circuits*, June 1984, pp. 100–105.
8. J. Ramirez-Angulo, R. L. Geiger and E. Sanchez-Sinencio, Characterization, evaluation, and comparison of laser-trimmed film resistors, *IEEE J. of Solid-State Circuits*, **SC-22**(6), 1987, pp. 1177–1189.
9. K. Schimmanz and A. Kost, Trim simulations of thin film resistors by the boundary element method (BEM), *Proceedings of the Conference on the Computation of Electromagnetic Fields (COMPUMAG)*, (July 2003).

Phillip Sandborn is a high school student at Wilde Lake High School in Columbia, Maryland. The work reported in this paper was performed as a science fair project in 2004 and later adapted for use in an undergraduate course at the University of Maryland. Phillip continued working on trimming embedded resistors in 2005 studying novel trimming patterns using experimental and simulation results.

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