Application-Specific Economic Analysis of Integral Passives in Printed Circuit Boards

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Abstract—This paper presents an application-specific economic analysis of the conversion of discrete passive components (resistors and capacitors) to integral passives that are embedded within a printed circuit board. In this study we assume that integral resistors are printed or plated directly onto wiring layers (as opposed to requiring a dedicated layer), that bypass capacitors, if present, are embedded by dielectric substitution into existing reference plane layers, and that singulated nonbypass capacitors, if present, are embedded using dedicated layer pair addition. The model presented performs three basic analyses.

1) **Board size analysis is used to determine board sizes, layer counts, and the number of boards that can be fabricated on a panel.**
2) **Panel fabrication cost modeling including a cost of ownership model is used to determine the impact of throughput changes associated with fabricating integral passive panels.**
3) **Assembly modeling is used to determine the cost of assembling all discrete components, and their associated inspection and rework.**

The combination of these three analyses is used to evaluate size/cost tradeoffs for several example systems including the NEMI hand-held emulator, a picocell board, and a fiber channel card.

Index Terms—Cost analysis, embedded passives, integral passives, technology tradeoff analysis.

I. INTRODUCTION

THE use of discrete passive components in electronic systems has continued to increase even as the degree of system integration has increased. While many people thought that discrete passives would be "integrated" away into integrated circuits, exactly the opposite has happened. In 1984, passive devices represented 25% of all components on printed wiring boards; by 1998 this fraction grew to over 90%, [1]. The demand for faster clock speeds, lower operating voltages, higher IO counts, and combined analog and digital functionality have all contributed to an increased demand for passive devices.

Why can't the increased demand for passive devices be met by fabricating passives within integrated circuits (ICs)? In fact, some passive devices are fabricated within ICs, however, designing passives into ICs would limit the IC's flexibility for

many uses, e.g., typically one IC is designed for multiple uses and the specific application it is used in is "tuned" with passives. In addition, real estate on an IC is usually more expensive than real estate on a board.

The trends above not only require more passives to be purchased and assembled into the system, but also suggest that discrete passives will consume increasing amounts of board area and assembly time. The electronics assembly industry has responded to the challenge by developing higher-speed chip shooters ($>100\,000$ placements/h are possible), and the passive components industry has responded by producing smaller passive components (0402, 40×20 mil passives are readily available today, with 0201, 20×10 mil components beginning to appear) [1].

An alternative solution to the passive growth trend is integrating multiple passives together within a single package (networks or arrays of passives). This approach can reduce assembly costs, however, the unit cost of integrated passives remains high (usually higher than the discrete passive components they replace). Even with the use of small dimension passives and judicious insertion of network or array passive components, many applications still cannot meet performance and size requirements. Integral passives (IPs) were introduced to address these needs. IPs are fabricated within substrates, and while IPs will never replace all passive components, they provide a potential advantage for many applications including

1) increased circuit density through saving real-estate on the substrate;
2) decreased product weight;
3) improved electrical properties through additional termination and filtering opportunities and shortening electrical connections;
4) cost reduction through increasing manufacturing automation;
5) increased product quality through the elimination of incorrectly attached devices;
6) improved reliability through the elimination of solder joints.

Potentially the biggest single question about integral passives is their cost, "$\cdots$ of all the inhibitors to achieving an acceptable market for integral substrates, the demonstration of cost savings is paramount" [2]. There is considerable controversy, however, as to whether the applications fabricated using integral passives will be able to compete economically with discrete passive technology. On the bright side, the use of integral passives reduces assembly costs, shrinks the required board size, and negates the cost of purchasing and handling discrete passive components. However, these economic advantages must be traded off against

the increased cost (per unit area) of boards fabricated with integral passives (a situation that will not disappear over time) and decreased throughput of the board fabrication process.

Section II of this paper discusses previous work on modeling the cost and size issues associated with integral passives and presents the analysis model used in this paper. One key element of the analysis model is the throughput of the board fabrication process with and without integral passives—Section III describes a model that uses throughput information to determine the profit margin required to justify the fabrication of integral passive boards on process lines that would otherwise be fabricating conventional boards. Section IV details analysis results for example applications.

II. MODEL DEVELOPMENT

The objective of the model developed and demonstrated in this paper is to capture the economic impact of the following competing effects when integrated passives are present in the board:

1) decreased board area due to a reduction in the number of discrete passive components;
2) decreased wiring density requirements due to the integration of resistors and bypass capacitors into the board;
3) increased wiring density requirements due to the decreased size of the board;
4) increased number of boards fabricated on a panel due to decreased board size;
5) increased board cost per unit area;
6) decreased board yield;
7) decreased board fabrication throughput;
8) decreased assembly costs;
9) increased overall assembly yield;
10) decreased assembly-level rework.

Due to the opposing nature of many of the effects listed above, the overall economic impact of replacing discrete passives with integral passives is not trivial to determine and, in general, yields application-specific guidelines instead of general rules of thumb. In fact the very nature of tradeoff analysis is one in which *the greater the detail necessary to accurately model a system, the less general and more application-specific the result*.

Several authors have addressed cost analysis for integral passives and thus provide varying degrees of insight into the economic impact of converting discrete passives to integral. The target of all these economic analyzes is to determine the effective cost of converting selected discrete passive components to integral components. The most common approach to economic analysis of integral passives is to

1) reduce the system cost by the purchase price and conversion costs[1] associated with the replaced discrete passives;
2) reduce the board size by the sum of the layout areas associated with the replaced discrete passives and determine the new number of boards on the panel;

3) determine the new board cost based on a higher per unit area cost for the integral passive panel fabrication and the new number-up computed in step 2.

The results of these three steps determine the new system cost. The effects included in this first-order approach are critical, however, the approach ignores several additional elements, most notably: decreased throughput for integral passive board fabrication means that board fabricators will have to use higher profit margins for integral passive boards to justify their production on lines that could otherwise be producing conventional boards; routing analysis of the board to determine not only what layers may be omitted, but what layers may have to be added to maintain sufficient wiring capacity as passives are embedded and the board is allowed to shrink; yield of both discrete passive components and the variation in board yield due to the integration of passives; and potential reductions in rework costs (due to both assembly defects and intrinsic functional defects) associated with discrete passives.

Brown [3] presents an outline of all the potential contributions to the life cycle cost of embedded passives. Brown then provides a quantitative evaluation similar to the process outlined above for digital and RF applications. Brown concludes that the more you integrate at the design level, the higher the likely cost savings and that in the applications considered by Brown, embedded passive allowed a possible savings that ranged from 27 to 73% over conventional implementations. Rector [2] provided the economic analysis that appeared in the 1998 NEMI Passive Component Technology roadmap [4] using the first-order approach outlined above. Rector concludes that integral passives can be economically feasible, but only if one considers more than the effects in the first-order model outlined above, but does not provide a quantitative analysis to support this supposition. Ohmega Technologies Inc. has also generated a cost model for assessing cost tradeoffs associated with it's Ohmega-Ply® integral resistor material, [5]. The Ohmega cost model follows the first-order approach described above, and includes yield and rework effects. Ohmega concludes that 2–4 embeddable resistors per in^2 are required to make the use of the Ohmega-Ply material economically practical.

The most detailed analysis to date is from Realff and Power [6]. Realff and Power developed a technical cost model for board fabrication and assembly. The model includes test (board and assembly), yield, and rework. The focus of the model is on the equipment requirements, under the assumption that integral resistors are fabricated using a dedicated resistor layer, they conclude that for integral resistors to have a significant impact on the cost of a system, their use must allow the removal of equipment or in some other way fundamentally change the assembly process (e.g., changing from double to single sided assembly). Only integral resistors are considered in [6]; Power *et al.* [7] extend the model in [6] to integral capacitors and cast it in the form of an optimization problem targeted at choosing which discrete passives to integrate based on an assumption of assembly and substrate manufacturing process details, and material properties.

Another analysis that recently appeared focused on design tradeoffs for a GPS front end, [8]. This analysis includes detailed

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[1]Conversion costs are the handling, storage and assembly costs associated with a discrete component.

cost modeling of thin-film integral resistors and capacitors performed using the modular optimization environment software tool from ETH.

In the model presented here, we incorporate quantitative routing estimation and assess board fabrication throughput impacts for setting profit margins on board fabrication, effects that have not been included in previous models. We also make different technology assumptions than were used in the analyses cited previously, i.e.,

1) Integral resistors are fabricated directly on wiring layers via printing or plating a resistive material directly on a wiring layer only where an integral resistor is required (e.g., [9], [10])—as opposed to requiring dedicated integral resistor layers as assumed previously, [5] and [6].
2) Bypass capacitors are embedded by dielectric substitution into an existing reference plane layer (as opposed to layer pair addition).
3) Singulated integral capacitors if present are fabricated via dedicated layer pair addition.

The remainder of this section describes a new model that incorporates these additional effects and allows size/cost tradeoff analysis for systems containing integral resistors and capacitors (integral inductors are not addressed in this work).

A. Board Size and Routing Calculations

As discrete passive components are converted to integral passives, the physical size of the board can either remain fixed or is allowed to optionally decrease by the layout area associated with the discrete passives given by

$$A_{\text{new}} = A_{\text{conv}} - \sum_{i=1}^{N} (l_i + S)(w_i + S) \qquad (1)$$

where
S minimum assembly spacing;
l_i and w_i length and width of the ith discrete passive;
N over all discrete passives that are converted to integral passives;
A_{conv} conventional board area.

We assume that if the board is allowed to shrink, its aspect ratio is preserved, thus, the new board length (L_{new}) and width (W_{new}) are given by

$$L_{\text{new}} = \sqrt{\frac{A_{\text{new}} L_{\text{conv}}}{W_{\text{conv}}}} \qquad (2a)$$

$$W_{\text{new}} = \frac{W_{\text{conv}}}{L_{\text{conv}}} L_{\text{new}} \qquad (2b)$$

where L_{conv} and W_{conv} are the length and width of the conventional board. If the board is double sided, the calculation in (1) and (2) can be performed independently for each side of the board, the larger of the two sides determines the new board size.

The area consumed by the integral passives on internal layers impacts the tradeoff analysis by decreasing the wiring available

on internal layers. The area occupied by an integral resistor on a board inner layer is given by

$$A_R = \begin{cases} \dfrac{0.75R}{r} m^2, & \text{for } 0.75R > r \\[2mm] \dfrac{r}{0.75R} m^2, & \text{for } 0.75R \le r \end{cases} \qquad (3)$$

where
R value of the resistor;
r resistivity of the resistor material (Ω/square);
m minimum feature size for integral resistor fabrication.
Since integral resistors are designed and fabricated to smaller (resistance) values than required and trimmed, a factor of 0.75 is included in (3), [11].

There are two types of capacitors that must be considered—bypass (decoupling) capacitors, and singular nonbypass capacitors. We assume that bypass capacitors can be absorbed into dedicated bypass layer pairs (planar distributed capacitance layers) and the nonbypass capacitors must be fabricated individually on a dedicated capacitor layer pair if they are to be embedded. The area occupied by an individual nonbypass integral capacitor on a capacitor layer pair is

$$A_c = \frac{C}{c} \qquad (4)$$

where C is the value of the capacitor, and c is the capacitance per unit area of the capacitor layer pair. Assuming square capacitors, the number of integral capacitor layer pairs (for nonbypass capacitors) required in the board is given by

$$N_{\text{integral cap layers}} = \left\lceil \frac{\sum_{j=1}^{N_c} \left(\sqrt{A_{C_j}} + S_c \right)^2}{A_{\text{new}}} \right\rceil \qquad (5)$$

where N_C is the total number of nonbypass capacitors that are converted from discrete to individual integral capacitors, and S_c is the effective spacing between individual integral capacitors on the integral capacitor layer pair. S_c is usually set larger than the minimum spacing possible to allow for perforation of the integral capacitor layer by vias and through holes, and to allow area for interconnection.

Besides estimating the physical size of the board after the integration of selected discrete passive components, we also need to consider the routing requirements. The following routing assumptions are made with respect to integral passives.

1) The IO (effectively the nets and vias) associated with discrete resistors that are embedded are effectively removed from the routing problem, i.e., the integral resistors are fabricated in series with the nets they are attached to on the wiring layers, however, the area occupied by the integral resistors blocks routing and is accounted for, see (7).
2) Non-bypass discrete capacitors converted to integral capacitors have no effect on the routing problem.
3) The IO (effectively the nets and vias) associated with discrete bypass capacitors converted to an integral capacitor are effectively removed from the routing problem.

With these assumptions and the routing information from the conventional implementation, the routing requirements, and thereby the number of layers required, for an implementation

that includes integral passives can be determined. An estimation of the minimum number of layers required to route the application proceeds as

$$N_{\text{layers}_{\text{new}}} = \frac{W_{\text{used}_{\text{new}}} + W_{\text{blocked}}}{W_{\text{layer}_{\text{new}}}} \left(\frac{U_{\text{conv}}}{U_{\text{limit}}} \right) \qquad (6)$$

where U_{limit} is the maximum fraction of the theoretically available wiring in the board that can be used for routing, and U_{conv} is the fraction of that wiring that is actually used to route the conventional application. The ratio of U_{conv} and U_{limit} measures the routing efficiency of the conventional implementation. When the ratio is large (i.e., close to one), the implementation has effectively used all the wiring that is available and any additional wiring would require the addition of another layer pair or an increase in board area. At some smaller value, any decrease in wiring would allow the omission of a layer pair.

The wiring blocked (W_{blocked}) by integral resistors (length of wiring that can not be used) is given by

$$W_{\text{blocked}} = \left(\frac{\sum_{i=1}^{N_R} A_{R_i}}{A_{\text{new}}} \right) \left(\frac{A_{\text{new}}}{A_{\text{conv}}} W_{\text{layer}_{\text{conv}}} \right) \qquad (7)$$

where

N_R number of integral resistors;
A_{new} (1);
A_R (3).

The second multiplier is the wiring per layer in the integral passive board with no integral resistors included ($W_{\text{layer}_{\text{new}}}$). The total length of wiring used for the new implementation is given by

$$W_{\text{used}_{\text{new}}} = f \left(W_{\text{used}_{\text{conv}}} \right) \qquad (8)$$

where f is the fractional change in required total wiring length. The wiring used in the conventional implementation is found from

$$W_{\text{used}_{\text{conv}}} = W_{\text{avail}_{\text{conv}}} \qquad (9)$$

where $W_{\text{avail}_{\text{conv}}}$ is the total length of wiring theoretically available in the conventional board ($W_{\text{layer}_{\text{conv}}}$ multiplied by the number of layers in the conventional board minus layers on which wiring is not done, e.g., reference planes). Assuming that the total wiring length required is proportional to the total number of system IO that require routing (a fundamental assumption in routing estimation approaches that compare requirements and resources, [12]), f is found from

$$f = \frac{N_{\text{IO}_{\text{new}}}}{N_{\text{IO}_{\text{conv}}}} \qquad (10)$$

where

$N_{\text{IO}_{\text{new}}}$ $N_{\text{IO}_{\text{conv}}} - 2N_R - 2N_{\text{BC}}$ total number of system IO in the new implementation (assuming 2 IO per resistor and capacitor), assuming resistors are printed directly onto wiring layers;
N_R number of integral resistors;
N_{BC} number of bypass capacitors absorbed into a bypass capacitance layer pairs;

$N_{\text{IO}_{\text{conv}}}$ total number of system IO in the conventional implementation.

Note, N in (1) is $N_R + N_C + N_{\text{BC}}$ where N_C is the number of nonbypass capacitors that are embedded into the board. The number of IO in the conventional implementation is given by

$$N_{\text{IO}_{\text{conv}}} = N_{\text{nets}_{\text{conv}}}(\text{fanout} + 1) \qquad (11)$$

where

fanout   average number of IO that a net attaches together minus one (assumed to be the same for the conventional and integral passives implementations);
$N_{\text{nets}_{\text{conv}}}$ number of nets in the conventional implementation.

Since layers occur in pairs in printed circuit board manufacturing, the result given by (6) is rounded up to the nearest multiple of two for use in the model. Note, the final value of $N_{\text{layers}_{\text{new}}}$ given by (6) is independent of $W_{\text{layer}_{\text{conv}}}$.

B. Cost Analysis

Using the size and routing relationships developed in the last section, we can predict the board fabrication costs. The price per conventional board is given by

$$P_{\text{conv}} = (1 + M_{\text{conv}}) \frac{C_{\text{layer pair}} A_{\text{conv}} N_{\text{layers}_{\text{conv}}}}{N_{\text{up}_{\text{conv}}}} \qquad (12)$$

where

M profit margin (see Section III);
$C_{\text{layer pair}}$ cost per unit area per layer pair;
$N_{\text{up}_{\text{conv}}}$ number up, number of boards that can be fabricated on a panel;
$N_{\text{layer}_{\text{conv}}}$ total number of layers (wiring and reference) in the conventional implementation of the board.

The $N_{\text{up}_{\text{conv}}}$ is computed from the board length and width, panel length and width, minimum spacing between boards, and the edge scrap allowance using the model in [13]. The price per integral passives board is similar to (12), with the addition of the capacitor layer costs (if integral bypass or nonbypass capacitors are present)

$$\begin{aligned} P_{\text{new}} = \frac{(1 + M_{\text{new}})}{N_{\text{up}_{\text{new}}}} \big[&C_{\text{layer pair}_{\text{new}}} \text{Area}_{\text{new}} N_{\text{layers}_{\text{new}}} \\ &+ N_{\text{bypass cap layers}} C_{\text{bypass cap layer}} \\ &+ N_{\text{integral cap layers}} C_{\text{integral cap layer}} \big] \end{aligned} \qquad (13)$$

where

$N_{\text{layers}_{\text{new}}}$ minimum number of layers required to route the application given by (6);
$N_{\text{integral cap layers}}$ number of integral capacitor layers given by (5);
$N_{\text{bypass cap layers}}$ number of bypass capacitor layers.

The new layer pair cost in (13) is given by

$$\begin{aligned} C_{\text{layer pair}_{\text{new}}} = C_{\text{layer pair}} + (C_{\text{resistor material}})(N_{\text{up}_{\text{new}}}) \\ \times \sum_{i=1}^{N_{R'}} \text{Area}_{R_i} + N_{R'} C_{\text{trim}} N_{\text{up}_{\text{new}}} + C_{\text{print}} \end{aligned} \qquad (14)$$

where the sum in (14) is taken over all integral resistors in the particular layer pair of interest $(N_{R'})$, and

$C_{\text{resistor material}}$ cost per unit area of the resistive material printed on the wiring layers to create integral resistors;

C_{trim} average cost of visiting one integral resistor for the purposes of trimming;

C_{print} average cost of printing or plating all integral resistors onto one layer pair.

The board price is combined with component-specific assembly, test, and rework costs to determine the system cost. The average effective cost associated with a single instance of a discrete passive (after [14]) is computed as follows:

$$
\begin{aligned}
C_{\text{discrete}} = {} & P_{\text{discrete}} + C_{\text{handling}} + C_{\text{assembly}} + C_{\text{AOI}} \\
& + (1 - Y_{\text{assembly}})(C_{\text{assbly rework}} + P_{\text{discrete}} \\
& + C_{\text{handling}}) + (1 - Y_{\text{functional}}) \\
& \times (C_{\text{func rework}} + P_{\text{discrete}} + C_{\text{handling}}) \quad (15)
\end{aligned}
$$

where

P_{discrete} purchase price of a discrete passive component;

C_{handling} storage and handling costs associated with a discrete passive component;

C_{assembly} cost of assembly of a discrete passive component (per site);

C_{AOI} cost of inspecting a discrete passive component (per site);

Y_{assembly} assembly yield for discrete passive components;

$Y_{\text{functional}}$ functional yield of discrete passive components;

$C_{\text{assbly rework}}$ cost of reworking an assembly fault (per site);

$C_{\text{func rework}}$ cost of diagnosing and reworking a functional fault.

The $(1 - Y_{\text{assembly}})$ term in (15) represents the fraction of discrete passives requiring rework (replacement) due to assembly faults. The $(1 - Y_{\text{functional}})$ term in (15) represents the fraction of discrete passives requiring rework (replacement) due to functional faults. Equation (15) assumes that all assembly and functional faults associated with discrete passives are diagnosable and reworkable.

The total system cost (for relative comparison purposes) is given by

$$
C_{\text{system}} = \sum_{i=1}^{N_{\text{discrete}}} C_{\text{discrete}_i} + P_{\text{board}} \quad (16)
$$

where

C_{discrete_i} cost associated with the ith discrete passive component from (15);

P_{board} board price from (12) or (13);

N_{discrete} number of discrete passive components assembled on the board.

Note, the following costs are not included in the formulation because they are assumed to be the same whether or not the system contains integral passives: all functional testing costs are ignored, all costs associated with other nonembeddable system components are ignored.

III. THROUGHPUT ANALYSIS

A fundamental issue that has not been addressed in previous cost analyses associated with integral passives is the throughput of the process that is used to manufacture the boards. Throughput is a measure of the number of products that can be produced in a given period of time, and is the inverse of the inter-departure time (the time elapsed between completed products). Throughput is key to understanding the profit margin that will be required to justify manufacturing integral passive boards. The objective of this portion of the analysis is the computation of application-specific relative profit margin values for conventional and integral passive versions of a board.

The situation faced by the board manufacturer may be the following: assume that there are two types of boards that could be fabricated on a process line, one is a conventional board with a known profit margin and the other is an integral passive board. To simplify the problem, assume that the number of boards to be manufactured will be the same for both types of board. The manufacturing cost of the integral passive board will be larger. Assuming the inter-departure time of the integral passive process will be longer than that for conventional boards, the manufacturer must decide what profit margin to use for the integral passive board so that the total profit per unit time made by selling integral passive boards equals or exceeds what can be made by selling the conventional boards. This is necessary to justify the use of a line to fabricate integral passive boards when it would otherwise be producing conventional boards.

To explore throughput effects and determine the relative profit margins of the printed circuit boards, a model has been developed that is similar to cost of ownership models for capital equipment (e.g., [15]). The model captures the costs due to maintenance (scheduled and unscheduled), yield loss, inter-departure time variations, and change overs.

The labor costs associated with scheduled and unscheduled maintenance, and change overs are given by

Scheduled Maintenance: $\quad L_{\text{sm}} = N_{\text{sm}} T_{\text{sm}} R_L \quad (17a)$

Unscheduled Maintenance: $\quad L_{\text{usm}} = \dfrac{\text{MTTR}}{\text{MTBF}}(T_{\text{total}}) R_L$

$\quad (17b)$

Change Overs: $\quad L_{\text{co}} = N_{\text{co}} T_{\text{co}} R_L \quad (17c)$

where

N_{sm} number of scheduled maintenance activities in a given period of time;

T_{sm} average labor time (touch time) associated with a scheduled maintenance activity;

N_{co} number of change overs in a given period of time;

T_{co} average labor time (touch time) associated with a change over;

R_L labor rate;

MTTR mean (labor) time to repair for an unscheduled maintenance event;

MTBF mean time between failures (unscheduled maintenance);

T_{total} total time in the period of interest.

We must now evaluate the throughput impacts of various critical manufacturing events. Computed throughput loss is basically determining lost opportunity costs, i.e., how much good product does not get manufactured because the process has been slowed or stopped, or because defective product is produced instead. We assume that scheduled maintenance does not affect the throughput, i.e., it is performed during periods when the process would not be operational, therefore, only the cost of performing the scheduled maintenance is important for our tradeoff, also we assume that the scheduled maintenance periods for lines producing conventional and integral passive boards are of the same length and occur at the same frequency. Note, if there is no effective off-shift (i.e., no time when maintenance can be performed that does not effect the throughput), then N_{sm} is set to zero and all maintenance is treated as unscheduled maintenance [16].

The throughput impact of process yield can be computed from the number of multilayer panels lost in a fixed time period due to process yield losses

$$\text{Lost}_{\text{yield}} = (1 - Y_{\text{ilp}})\frac{N_{\text{inner layers}}}{N_{\text{inner layers per board}}} \quad (18)$$

where

Y_{ilp}	yield of the panel inner layer process;
$N_{\text{inner layers}}$	number of panel inner layers produced in a fixed time period;
$N_{\text{inner layers per board}}$	number of inner layer pairs in a single board.

Unscheduled maintenance, assuming it is performed during time when the process line would otherwise be producing good product contributes the following lost time:

$$\text{Lost}_{\text{usm}} = (\text{MTTR} + 2T_{\text{c/s}})\frac{T_{\text{total}}}{\text{MTBF}} \quad (19)$$

where $T_{\text{c/s}}$ is the cool down/startup time associated with the line being stopped for the unscheduled maintenance activity. Similarly, the change overs result in lost opportunity to produce products

$$\text{Lost}_{\text{co}} = N_{\text{co}}(T_{\text{co}} + 2T_{\text{c/s}}). \quad (20)$$

Knowing the inter-departure time, the average number of multilayer boards that can be obtained from the process line during the time period defined by T_{total} is given by

$$N_{\text{boards}} = \left\lceil \frac{T_{\text{total}}}{T_{\text{inter}}N_{\text{inner layers per board}}} \times \left(1 - \frac{\text{Lost}_{\text{usm}} + \text{Lost}_{\text{co}}}{T_{\text{total}}}\right) - \text{Lost}_{\text{yield}} \right\rceil \times N_{\text{boards per panel}} \quad (21)$$

where

T_{inter}	interdeparture time of the inner layer process (time/inner layer pair);
$N_{\text{boards per panel}}$	number up, i.e., the number of boards that can be fabricated on a panel.

The parameter that needs to be evaluated for comparison purposes is the total profit in a fixed period of time from fabricating
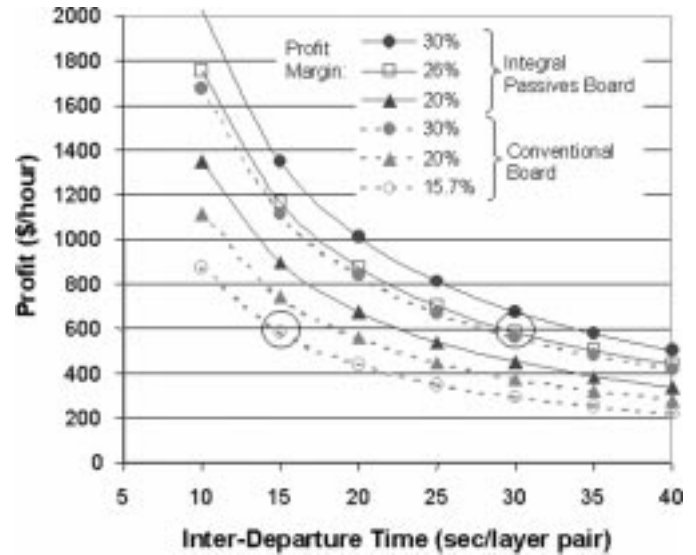

Fig. 1. Relationship between profit margin and production inter-departure time for conventional and integral passive board fabrication.

a specific board type. Note, the profit per board is not a good comparison metric because it does not account for the number of boards that are produced. The average profit in the time period associated with the constituent variables is computed from

$$\text{Average Profit} = N_{\text{boards}}V - (L_{\text{sm}} + L_{\text{usm}} + L_{\text{co}}) \quad (22)$$

where the value of a board (V) is given by

$$V = (1 + M)C_{\text{board}} \quad (23)$$

where

M	profit margin;
C_{board}	manufacturing cost per board.

The example results shown in Fig. 1 were generated using the model described by (17)–(23). If inter-departure times of inner layer production for conventional and integral passive layers, and the average profit margin for conventional boards are known, then the minimum required profit margin for integral passive board fabrication can be determined. Note, this cost model must be repeated for each board manufacturing scenario since the number of layers in the multilayer board and the dimensions of the individual board are application-specific.

The example shown in Fig. 1 indicates that if, conventional boards have a 15.7% profit margin and 15 s inter-departure time (per layer pair), then 30 s per layer pair integral passive board production is only feasible for profit margins of 26% or more. The most important conclusion from this analysis is the difference between the profit margins, the tradeoff analysis results are much less dependent on the absolute values of the profit margins. We consistently observe profit margin differences of ~10%. The analysis presented in Section IV assumes profit margins that make the average profit per hour of each type of board fabrication equal.

IV. ANALYSIS RESULTS

In this section we present the results of size/cost tradeoff analyzes performed on several different single board applications,

TABLE I
PICOCELL BOARD, HAND-HELD EMULATOR AND FIBER CHANNEL CARD APPLICATION CHARACTERISTICS

	Picocell Board	Hand-Held [16]	Fiber Channel Card
Number of Embeddable Discrete Resistors	27 (< 100 Ω) 19 (100-1000 Ω) 22 (1 – 10 kΩ) 1 (10 – 100 kΩ) 1 (>100 kΩ)	40 (<100 Ω) 134 (0.1 – 1 kΩ)	210 (< 100 Ω) 181 (100-1000 Ω) 150 (1 – 10 kΩ) 63 (10 – 100 kΩ) 6 (>100 kΩ)
Size of Embeddable Discrete Resistors	69 0805 (80x50 mils) 1 1201 (120x100 mils)	0402 (40 x 20 mils)	561 0603 (60x30 mils) 10 0805 (80x50 mils) 31 120x60 mils 8 250x120 mils
Number of Embeddable Discrete Capacitors	1 (< 100 pF) 29 (100 – 1000 pF) 13 (1 – 10 nF)	69 (<100 pF) 40 (100 - 1000 pF)	88 (0.001μF) 38 (0.01μF) 116 (0.1μF)
Size of Embeddable Discrete Capacitors	0805 (80x50 mils)	0402 (40 x 20 mils)	159 0603 (60x30 mils) 82 0805 (80x50 mils)
Discrete Passive Cost	$0.0045 per part	$0.0045 per part	$0.0045 per part
Conversion Cost (excluding assembly)	$0.015 per part	$0.015 per part	$0.015 per part
Board Size	2.27 x 6.87 inches	30 cm^2 (square board assumed)	12 x 18 inches
Number of Board Layers	10	6	12

TABLE II
DATA ASSUMPTIONS USED IN THE MODELING

Panel Fabrication	Throughput Analysis	Integral Passives
Panel size = 18 x 24 inches (except where otherwise noted)	Change overs = 4/week	Capacitance layer:10 nF/cm^2
Edge scrap = 0.75 inches	Change over time = 15 minutes	Resistive material: 200 ohms/square
Min. spacing between boards = 0.15 inches	Cool down and start up = 30 minutes	Minimum feature size for integral components = 15 mils
Cost per layer pair = $12.50/ft^2	MTBF = 200 hours (conventional) MTBF = 150 hours (integral passive)	$C_{resistor\ material}$ = $0.08/in^2
	MTTR = 1 hour	C_{trim} = $0.002/integral resistor
Assembly	Labor rate (repair) = $25/hour	C_{print} = $7.43/layer pair
Min. Assembly Spacing = 20 mils	Production hours = 5000/year	Cost of capacitor layer material = $14.40/ft^2 (>10 nF/in^2)
Yield = 0.992/discrete passive [5]		Spacing between non-bypass integral capacitors (S_c) = 50 mils
Cost = $0.0045/discrete passive	**Routing Analysis**	
AOI = $0.0001/discrete passive	Average fanout = 2.1	
Assembly Rework = $4/site [5]		
Functional Rework = $4/site [5]		

including a picocell board, the NEMI hand-held emulator and a fiber channel card. It is not the intent of these analyses to prove that integral passives lead to less expensive systems, rather we wish to understand the economic realities should we decide to use integral passives.

The relevant characteristics of the applications are given in Table I. The common data assumptions for both applications are shown in Table II.

A. Picocell Board Application

Fig. 2 shows analysis results for the picocell board as discrete resistors are replaced by integral resistors (capacitors are not integrated in Fig. 2). Relative system cost is plotted in Fig. 2 and throughout this section indicating the system cost less the cost of all nonembeddable components and functional testing. The specific solution (data points) in Fig. 2 indicate that the integral

passive board becomes economical when approximately 10% of the embeddable discrete resistors are embedded[2]. The data point at $18.00 is the relative cost of the system when the first resistor is embedded.

The resistor results appear as a "band" in Fig. 2 due to the range of values that U_{conv}/U_{limit} can take on in (6). The upper edge of the band (the closed data points in Fig. 2), represents the assumption that the conventional board used all available routing resources efficiently, i.e., U_{conv}/U_{limit} is close to 1.0. The lower edge of the band (the open data points in Fig. 2), represents the assumption that the conventional board made poor use of the available routing resources, i.e.,

[2]The integral resistors considered in this study are considerably more economical than integral resistors in previous studies due to the assumption of fabrication of the integral resistors directly on wiring layers as opposed to dedicated integral resistor layer.
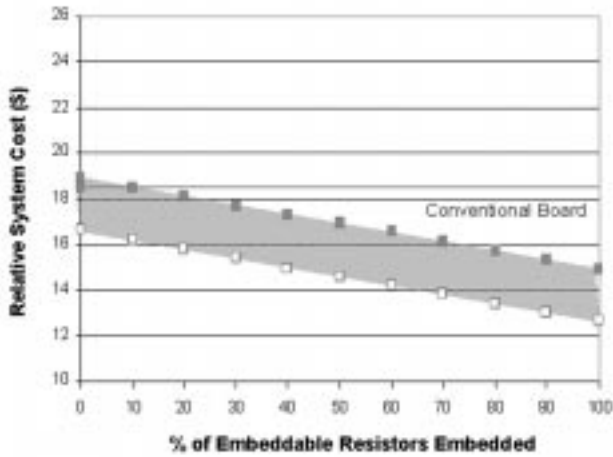
Fig. 2. Economics of integral resistors for the picocell board application. Each data point represents the integral passive solution for a specific routing resource assumption (assumption of the ratio of resources actually used to route the conventional implementation of the board and the theoretical maximum amount of resources that could be used), the band represents all possible integral passive solutions for this application; the solid horizontal line is the system cost of conventional implementations. Only resistors ≤ 10 KΩ were considered embeddable.
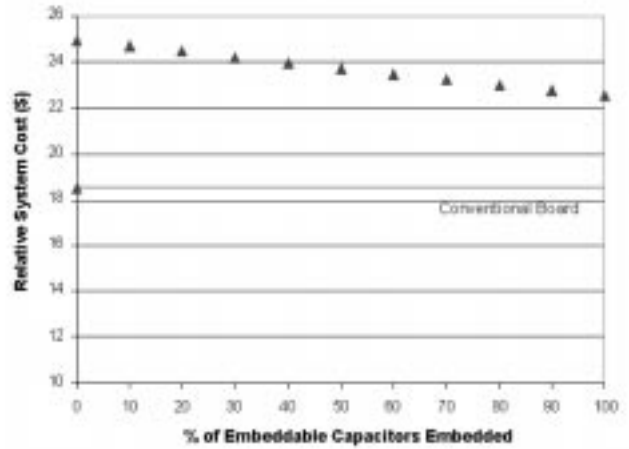

Fig. 4. Capacitor embedding for the picocell board application. Only capacitors ≤ 100 nF were considered embeddable.

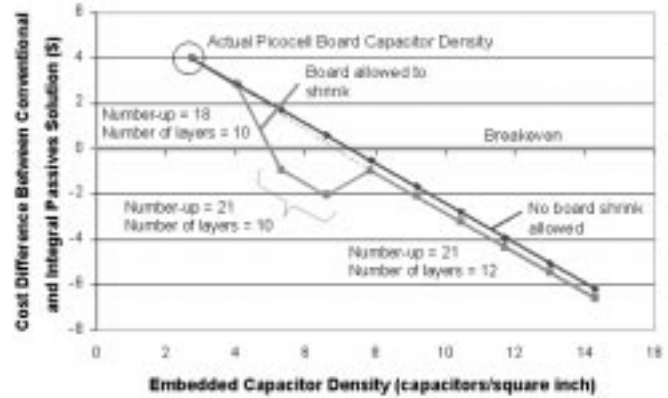Fig. 3. Board size decrease with resistor embedding for the picocell board application.

Fig. 5. Impact of embeddable capacitor density on system cost for the picocell board application. When the density of embeddable bypass capacitors is increased, the number up first decreases due to the decreased board size (if board size is allowed to change), and later (as density increases) a layer pair addition is required to support routing requirements of the application with the smaller board size.

$U_{\mathrm{conv}}/U_{\mathrm{limit}}$ is smaller.[3] Practically speaking, all solutions start at the top edge of the band (10 layers for the picocell board) and may step down to the lower edge of the band (8 layers for the picocell board) at some point depending on the actual value of $U_{\mathrm{conv}}/U_{\mathrm{limit}}$ for the application. Another type of step discontinuity can also appear in the results if the board shrinks in size enough so that more boards can be fabricated on a panel. In the picocell board case, the board size never decreases sufficiently to allow more boards to be fabricated on an 18×24 in panel, however, potential board size decreases

are still important to the customer and Fig. 3 shows the board area change as fraction of integral resistors is varied.

Next consider the integration of capacitors. Fig. 4 shows the relative system costs as the embeddable capacitors are embedded (none of the embeddable discrete resistors are embedded in Fig. 4). Since embedding of bypass capacitors requires material replacement and nonbypass capacitors requires the addition of an extra layer pair (for the technologies we assumed), the very first bypass capacitor embedded increases the cost of the board dramatically, but as more capacitors are embedded, the added cost of the replacement material layer is gradually offset by the avoidance of discrete capacitor part and assembly costs. The driver that determines whether capacitor embedding is economical or not, is the density of embeddable discrete capacitors on the board. Fig. 5 shows that if additional embeddable capacitors were added to the picocell board application (thus increasing the capacitor density), bypass integral capacitors would become economically viable
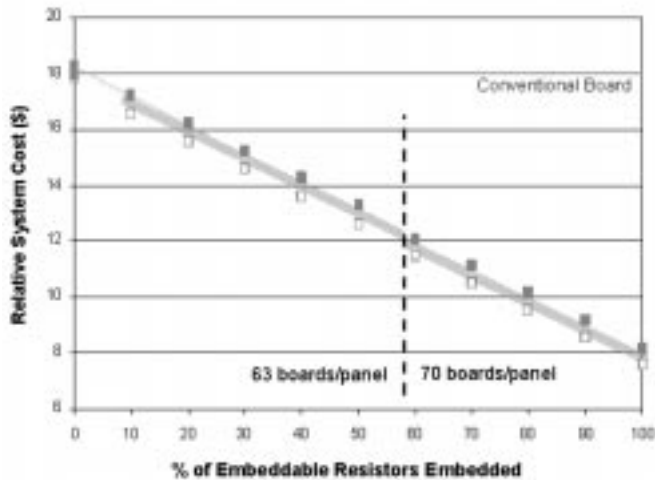
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[3]The minimum value is determined by finding the smallest value of $U_{\mathrm{conv}}/U_{\mathrm{limit}}$ that predicts the correct number of layers in the conventional solution.

Fig. 6. Economics of integral resistors for the NEMI hand-held product sector emulator (5.5×5.5 cm board fabricated on an 18×24 in panel). The data points represent specific integral passive solutions; the solid horizontal line is the relative system cost of the conventional implementation.

Fig. 7. Capacitor embedding for the 5.5×5.5 cm NEMI hand-held product sector emulator. No embedded resistors are fabricated in this example. The baseline for this plot (the horizontal line) is the board with none of the embeddable capacitors embedded.

at approximately 6.9 capacitors/in^2, whereas the actual picocell board application has only 2.76 capacitors/in^2.

B. NEMI Hand-Held Product Sector Emulator

Analyses similar to those performed for the picocell board have been applied to the NEMI hand-held emulator described in Table I. Fig. 6 indicates that the integral passive board becomes economical when approximately 3% of the embeddable discrete resistors are embedded. A discontinuity in the integral passive board data is labeled on the plot. The discontinuity appears when enough resistors have been embedded to sufficiently reduce the board size so that additional boards can be manufactured on the panel (number-up increases). In the hand-held emulator case, the boards are small (i.e., the number-up on the panel is large) and the overall price of the boards is low (~$2/board), therefore the effect of increasing the number-up has a minimal effect on the system cost.

Fig. 7 shows the relative system costs as the embeddable capacitors are integrated (none of the embeddable discrete resistors are embedded in Fig. 7). When bypass capacitors are embedded, the cost initially increased by the material replacement cost. We have assumed that when a bypass capacitance layer pair is added, less total bypass capacitance will be necessary[4], [17]. Note, a much better economic case can be made for integral bypass capacitors in the hand-held emulator than for the pico-cell board due to the larger embeddable bypass capacitor density (23.44 capacitors/in^2). Similar to the integral resistor characteristics, eventually enough bypass capacitors are embedded to reduce the size sufficiently to allow a number-up increase (note, there are fewer embeddable capacitors than resistors, so the this discontinuity occurs later in the embedding process than for resistors). Also note that a second discontinuity appears in

Fig. 8. Economics of integral resistors for the fiber channel card. The data points represent integral passive solutions. The solid horizontal lines are relative system costs of conventional implementations.

Fig. 7—a layer change. As board area decreased, so did the available wiring resources, eventually an additional layer pair had to be added to interconnect the system components.

C. Fiber Channel Card

Figs. 8 and 9 show the results of embedding resistors and bypass capacitors into the fiber channel card described in Table I. In this case the board is large and only one can be fabricated per panel (results for two different panel sizes are considered in Figs. 8 and 9). Because all the cost associated with fabricating integral resistors on a panel has to be born by a single board, 25–35% of the 610 embeddable resistors need to be embedded to realize a cost savings.

Fig. 9 shows the effect of integrating bypass capacitors for the fiber channel card. For this example there are only 242 embeddable capacitors on a 12×8 in board (1.12 embeddable capacitors/in^2). As indicated in the hand-held and picocell

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[4]At frequencies above a few MHz, the connection inductance of surface-mounted capacitors limits their effectiveness. For this reason, the amount of embedded capacitance required to achieve a given level of switching noise suppression may be significantly less than the total surface-mount capacitance it replaces.
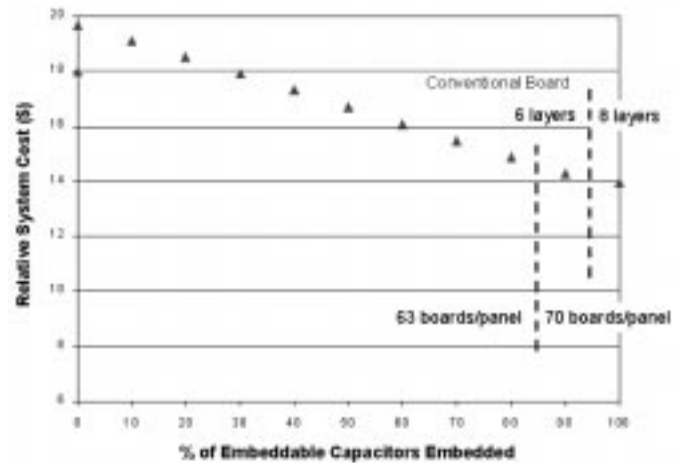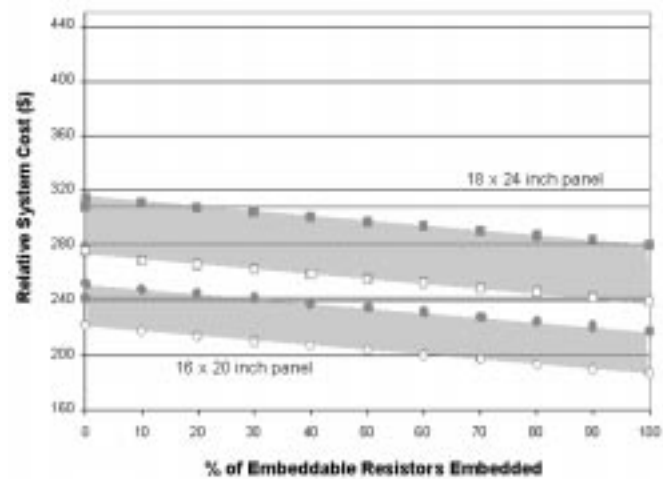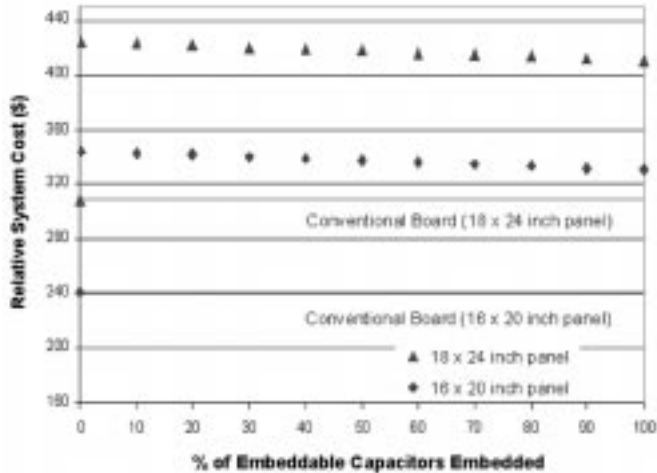
Fig. 9. Capacitor embedding for the fiber channel card. Note, in this case there are no embeddable discrete nonbypass capacitors.
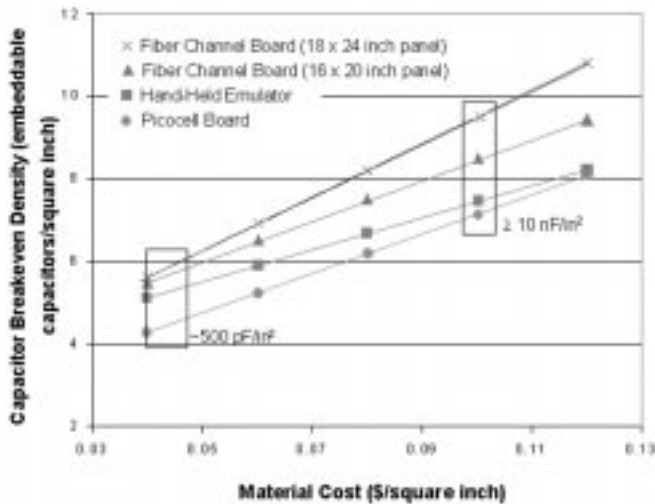

Fig. 10. Bypass capacitor breakeven densities as a function of dielectric material replacement costs. Only single layer substitution is considered in this plot. The actual capacitor densities: fiber channel board—1.12 caps/in^2, picocell board—2.76 caps/in^2, NEMI hand held emulator—23.44 caps/in^2.

examples, with such a low embeddable capacitor density it is not likely to be economical to embed the capacitors.

The economics of integral capacitors can be generalized by observing the application-specific embeddable capacitor density necessary to breakeven on costs, i.e., by plotting the embeddable capacitor densities where the cost difference between the conventional and embedded passive implementations is zero (for the picocell board application this point is 6.9 embeddable bypass capacitors per in^2 from Fig. 5). Fig. 10 shows the general result for the three applications considered in this paper. The critical assumptions for this plot are: the board size and the number of layers required for routing is not allowed to change. The one differentiator between the applications as far as this plot is concerned is the panelization efficiency (the total board area on the panel divided by the panel area). The dielectrics used to produce integral capacitor layers are relatively expensive and

would be purchased and used at the panel size, therefore, a low panelization efficiency indicates that the application is wasting a lot of the expensive material, versus a larger panelization efficiency indicates less waste and therefore lower breakeven capacitor densities are possible. This effect can be clearly demonstrated for low layer pair costs ($5 - 8/ft^2$), but is less pronounced for higher layer pair costs($> 10/ft^2$).

V. DISCUSSION AND CONCLUSIONS

In this paper we have presented the results of an application-specific economic analysis of the conversion of discrete passive components (resistors and capacitors) to integral passives that are embedded within a printed circuit board. The model has been demonstrated on a picocell board, the NEMI hand-held emulator, and a fiber channel board. In these cases, we found integral resistors to be generally cost effective with the most significant economic impact resulting from either number-up increases due to board size reductions, or layer count decreases due to reductions in routing requirements. Because we considered integral resistors fabricated directly on wiring layers (as opposed to dedicated integral resistor layers assumed in previous studies [5] and [6]), we can not generalize to components per unit area because the results are driven by the board fabrication profit margin (profit margin is a fractional increase in board cost and thus much smaller in absolute terms for high number-up), whereas cost reduction is through omission of discrete part costs. As expected, when a technology that adds resistors directly to the wiring layers is used, integral resistors become economically viable when considerably fewer are integrated than for layer addition technologies.

For the applications considered, integral bypass capacitors become economical when the embedded capacitor density (number of discrete capacitors/in^2) reaches 7–8.5 capacitors/in^2 or greater for reasonable panelization efficiencies when the dielectric replacement material with a cost of $0.10/in^2 is assumed (these densities decrease if less expensive dielectrics can be used).

It must be reiterated that due to the opposing nature of many of the effects outlined in this paper, the overall economic impact of replacing discrete passives with integral passives, in general, yields application-specific results instead of general rules of thumb. We also need to point out several factors that should be kept in mind when interpreting the results in this paper.

1) Several system implementation details are not addressed in this analysis including the following.

   a) Waste disposition in board fabrication—we only account for additional waste disposition costs associated with the fabrication of integral passive boards in the profit margin differential.

   b) Non-homogeneous panelization—some panel fabrication technologies and materials allow boards to be laid out on the panel with 90 degree relative rotations resulting in the potential for more boards on a panel, we have assumed homogeneous panelization in this analysis.

   c) We have not considered the possibility raised in [2] that the conversion of discrete to integral passives

may allow some double-sided assemblies to become single sided thus saving significant assembly costs.

2) With any tradeoff analysis, the results are only as good as the input data, i.e., inaccuracies in the input data will change the results of the analysis. The software implementation of the methodology described in this paper uses Monte Carlo analysis to model the impact of data input uncertainties.

3) In addition to the direct effects on system cost discussed in this paper, there are many other "life cycle" effects on the system cost. These effects include the changes in the system reliability, performance, end-of-life options and the design overhead that constitute effective life cycle costs. For some systems, integral passives may also affect the upgradability and field repairability of the system.

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