An Assessment of the Applicability of Embedded Resistor Trimming and Rework*

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***Abstract* – The successful use of embedded resistors in many applications will require that the fabricated resistors be trimmed prior to lamination into printed circuit boards to attain required design tolerances. Depending on the application, the economic value of the board being fabricated, and the process used to create the embedded resistors, it may also be prudent to consider reworking resistors that are incorrectly trimmed or with initial values that are too large (un-trimmable resistors). This paper uses a model of the resistor/board yield coupled with a cost model of the trim and rework processes to identify conditions under which applications should neither trim nor rework, trim but not rework, or perform both trimming and rework of embedded resistors, as a function of the design tolerance for the resistors and the accuracy with which the embedded resistors can be formed. Example results are presented for several applications ranging from small boards with a high density of embedded resistors to large boards with a low density of embedded resistors. Distinct regions of trimming and rework applicability that are nearly application independent can be identified as a function of design tolerance, printing/plating/etching variation, and the characteristics of the trimming process.**

***Index Terms* – Embedded passives, integral passives, embedded resistors, laser trimming, rework, cost analysis.**

I. INTRODUCTION

Embedding passive components (capacitors, resistors and possibly inductors) within printed circuit boards is one of a series of technology advances enabling performance increases, size and weight reductions, and potentially cost advantages in the manufacturing of electronic systems [1]. There are many factors associated with how and

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when to include embedded passives in systems. In general the decisions require application-specific size/cost/performance tradeoff analyses and are rarely simple, [2].

One significant factor governing the applicability of embedded resistors is their tolerance level. The tolerance to which a resistor can be fabricated determines the applications for which it can be used and potentially affects its yield impact on the application. Tolerances of ±10% or larger are readily achievable with today's technologies, however, achieving ±1% is a challenge, [3]. While surface mount resistors can be pre-sorted by value, or even replaced during assembly when their value is not within the required range, embedded resistors provide no such opportunity and must be within design tolerance value before the board fabrication process is completed. One possible impediment to the widespread use of embedded resistors is the ability and expense of tuning or trimming the resistors to the value range defined by the design tolerances prior to the lamination of the layer pair containing them into the board, [4].

A. Laser Trimming of Embedded Resistors and Rework

Laser trimming of film resistors has been performed for many years with application to resistors on silicon and trimming of surface mount discrete resistors prior to packaging, e.g., [5]. However, only recently, highly automated laser trimming technologies have been developed and demonstrated for trimming of embedded resistors during the board fabrication process, [3]. Resistors are normally trimmed by micromachining a trough in the resistive element. The length and path-shape of the trough determine the resistance change obtained. Several different path-shapes can be used depending on the specific trimming requirements. As the laser cuts the trough, the resistor value is measured and used as feedback to control the trimming process.

It is also possible to consider reworking embedded resistors prior to completion of the board fabrication process. Resistors may be reworked because their value is too large due to either trimming errors or original fabrication (laser trimming can only increase the resistance of a resistor, not decrease it). Trimming errors are most commonly due to material inconsistencies, i.e., if a void in the embedded resistor material is encountered during the trimming process, the resistance value may "jump" when the trimming trough reaches it. One method of reworking embedded resistors is to print conductive ink on the surface of an embedded resistor thus adding a lower value parallel resistor that effectively "trims down" the resistor value, [6].

Unfortunately, trimming and rework equipment is expensive and both processes potentially represent bottlenecks in the board fabrication process. Therefore, the question naturally arises as to under what conditions (application properties and resistor fabrication process) should trimming and possibly rework be performed versus disposal of the boards or layer pairs or boards that do not meet design specifications?

II. Resistor Fabrication Process Distributions and Trimming

When resistors are fabricated the resulting values form a distribution, Fig. 1a. If the resistors are to be trimmed, the fabrication target resistance (peak of the distribution) is below the application target resistance so that the greatest number of fabricated resistors can be trimmed to values within the specified range. Figure 1b shows a generalized distribution of fabricated resistors of a particular value with the fabrication target and application targets. The High Specification Limit (HSL) and the Low Specification Limit (LSL) are determined from the design tolerance associated with the resistor. The area under the curve between the HSL and the LSL represents the yield of the untrimmed resistor. The lower limit of the ability to successfully trim a resistor is approximately 55% of the application target [7]. The area under the curve between the lower trimming limit (L) and HSL represents the yield of trimmed resistors (assuming no trimming defects). Resistors in the distribution that have values below the lower trimming limit (L) or above HSL would generally be considered yield loss (unusable and un-trimmable). Rework

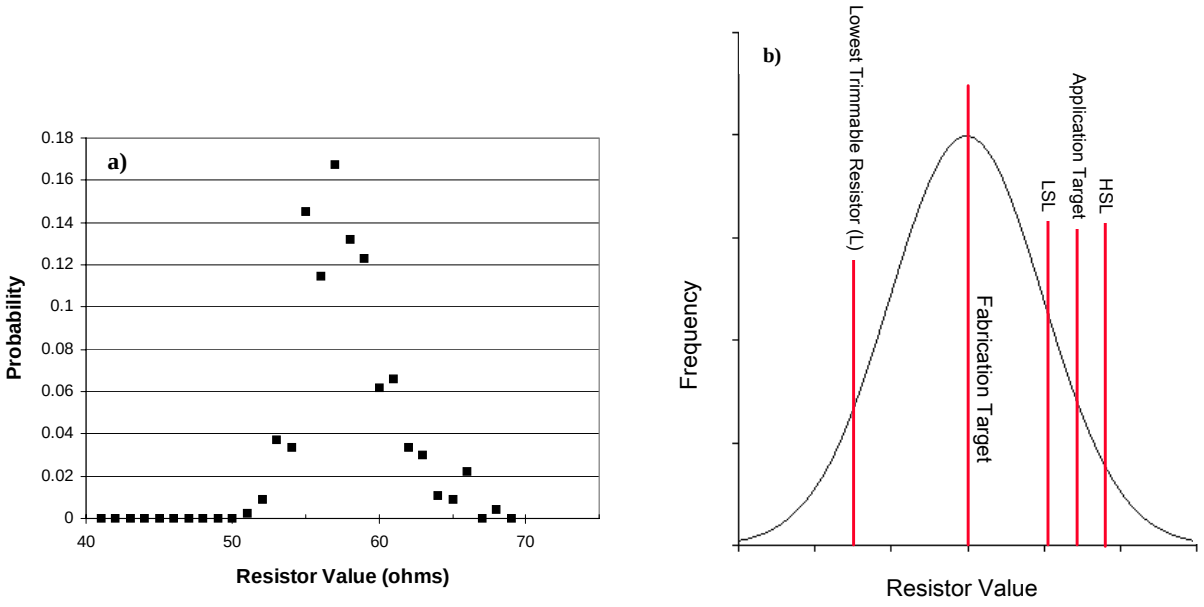

Fig. 1 – Distribution of fabricated resistors: a) experimentally determined [3], b) generalized distribution model.

allows the resistors above HSL to be recovered and used. In cases where no trimming is planned, the process would be centered so that the fabrication target and the application target are the same.

In order to determine the yield of the trimming process, we assume a centered trimming process defined by a normal distribution where resistor yield after trimming is the area under the probability distribution between the HSL and LSL of the trimming process. Note, here we are not referring to the distribution of the fabricated resistors (Fig. 1), but the distribution associated with the trimming process. The process capability index, C_{pk} for a process described by a symmetric distribution, is HSL-μ divided by 3σ (where μ and σ are the mean and standard deviation of the trimming process). The resulting yield is shown in Fig. 2.

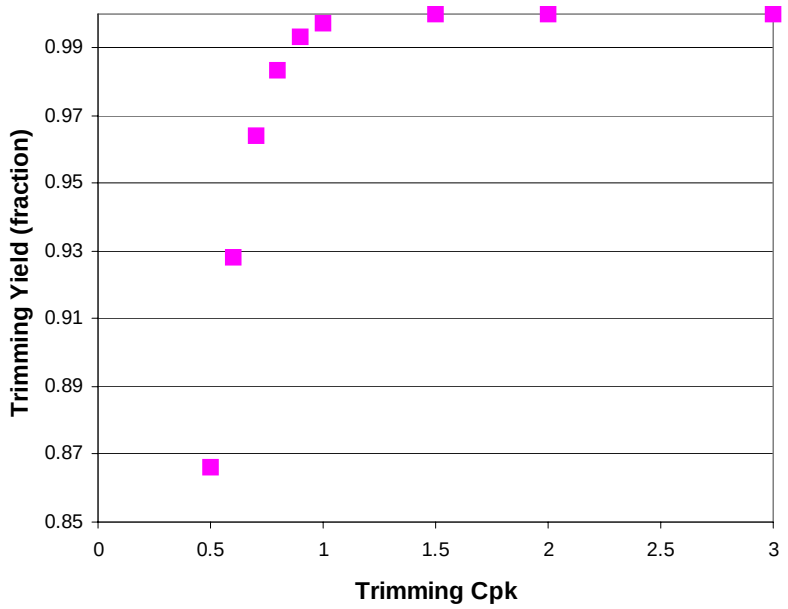

Fig. 2 – Relationship between the C_{pk} of the trimming process and the trimming yield.

The C_{pk} of the trimming process for 1% design tolerance resistors has been found to be 1-4 and for 5% design tolerance resistors is 5-20, [7]. In the analysis presented in Section IV, we assume that C_{pk} = (3)(design tolerance in %) as a baseline. The sensitivity of the analysis to trimming yield will be treated in Fig. 11 and its associated discussion.

III. Model Description and Assumptions

To date, modeling of the resistor trimming process has been limited to modeling the electrical characteristics of the resistor with various trimming paths and shapes, e.g., [8], [9]. In this paper a cost model for the trimming and

rework process for embedded resistors is applied to several embedded passive board examples to determine the conditions under which resistors should be trimmed and possibly reworked. This section provides an overview of the model developed for this work.

The objective of the model developed and demonstrated in this paper is to enable the determination of the economical regions for:

- No trimming and no rework (assuming a centered process);
- Trimming and no rework;
- Trimming and rework.

The above regions are determined as a function of the application-specific design tolerance and the accuracy with which features on the embedded resistor layer can be fabricated, i.e., either variations in the fabrication of the resistor terminal separation, the resistor material shape, and/or the material resistivity (or thickness). These variations apply to both dedicated layer pair resistors approaches, e.g., Ohmega-Ply® [10] or Gould™ [11], with which the actual embedded resistors are formed subtractively through etching, or additive processes such as the MacDermid M-Pass™ technology, [12].

A combination of several models must be used to perform the desired analysis. A summary of the complete analysis is shown in Fig. 3. The application-specific inputs to the model are the quantity and design tolerance of each different value of resistor to be embedded, plus the board dimensions. Table I shows the general assumptions used in addition to the application-specific information.

TABLE I – GENERAL MODELING ASSUMPTIONS

C_{pk}	Set equal to three times the design tolerance in %
Panel width	18 inches
Panel length	24 inches
Edge scrap on panel	0.75 inches
Minimum spacing between boards on panel	0.15 inches
Layer pair interdeparture time (T_i) – effective time interval between layer pairs in the manufacturing process	35 sec
Fraction of layer pairs that are embedded resistor layer pairs (f_r)	0.1

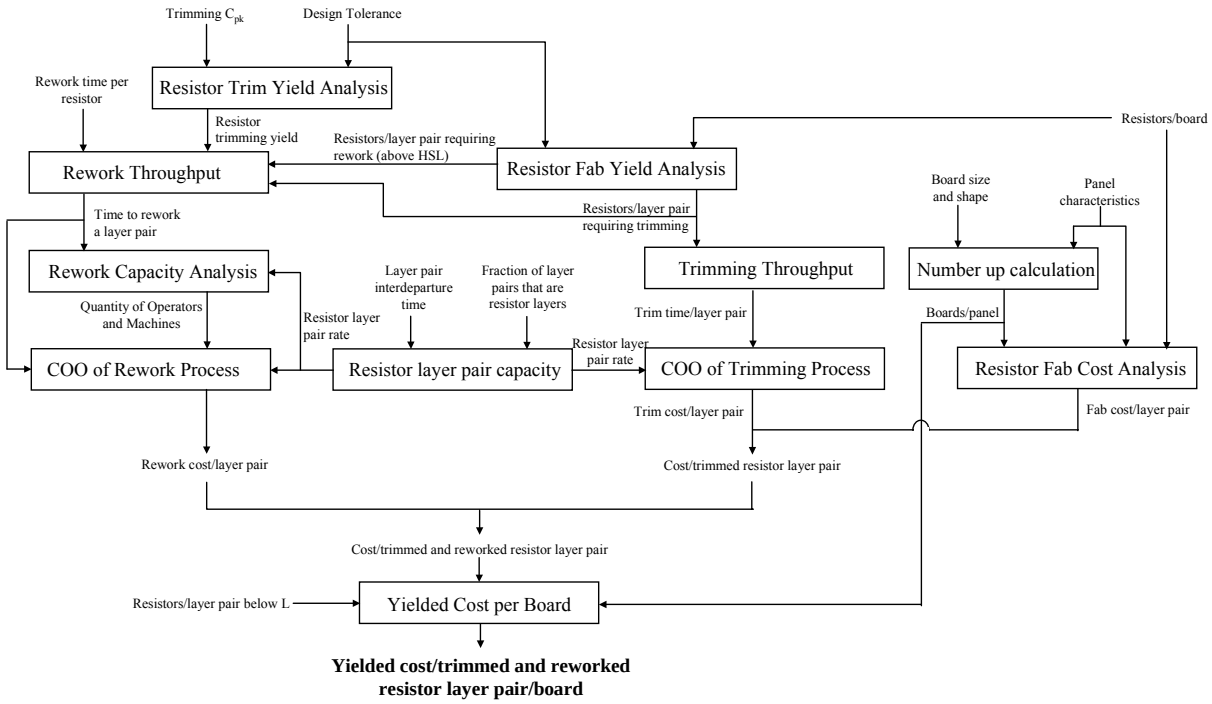

Fig. 3 – Summary of cost analysis process.

To start the modeling process, the number of resistors per layer pair that require trimming is determined (see subsection B). Using a laser trimming throughput model developed by ESI [13], the amount of time to trim a layer pair is computed as a function of the number of resistors to be trimmed per layer pair and the size of the panel. The trimming time per layer pair is an input to the Cost of Ownership (COO) model of the trimming process. The resistor design tolerance and assumptions about the C_{pk} of the trimming process are used to determine the yield of the trimming process (see Section II).

Using the yield of the trimming process, the rework time per resistor and the number of resistors that need to be reworked, the average rework time per layer pair is computed using,

$$T_{rl} = (N_{r1} + N_{r2})T_r + T_{rs}, \quad (1)$$

where

N_{r1} = number of resistors per layer pair above HSL (derived in subsection B)

N_{r2} = number of resistors per layer pair that require rework due to trimming errors (derived in subsection B)

T_r = rework time per resistor

T_{rs} = rework setup time (load and unload) per layer pair.

The number of operators and machines required for rework is computed from the average time to rework a layer pair and the rate at which layer pairs that requiring trimming will be produced. The rate at which resistor layer pairs are produced is given by,

$$r_r = \frac{f_r}{T_i}, \tag{2}$$

where f_r and T_i are defined in Table I. The number of rework equipment setups (machines) necessary so that rework is not a bottleneck is given by (assuming that a fractional number of machines is not possible),

$$N_{rs} = \lceil T_{rl} r_r \rceil. \tag{3}$$

In the case of a manual rework process, N_{rs} represents the number of people necessary (we assume one equipment setup per person), and the operator utilization is given by $T_{rl}r_r$. If the rework process is automated, N_{rs} represents the number of machines (a fixed operator utilization given in Table II is assumed). We also consider a "mixed" rework case in which rework needs are satisfied by the manual process until 50% or more of the capacity of the automated equipment can be used (similarly, the first automated machine is supplemented with the slower manual process until at least 50% of the capacity of a second automated machine can be used, etc.).

We also need to compute the average fabrication cost of a resistor layer pair. A general relation for the average cost of a layer pair containing embedded passives is given by (4) (note, by setting various terms to zero, one can represent the cost of either subtractive dedicated layer pair approaches, e.g., Ohmega-Ply or Gould, or additive approaches that fabricate the embedded resistors directly on wiring layers),

$$C_{rl} = C_c A_l + N_r C_r + C_l. \tag{4}$$

where

C_c = cost per layer pair per unit area (conventional layer pair)

A_l = area of the layer pair (panel)

N_r = number of embedded resistors in the layer pair

C_r = cost per embedded resistor

C_l = extra cost per embedded resistor layer pair.

The number of embedded resistors per layer pair is the number of embedded resistors per board multiplied by the number of boards on the panel (number up, N_{up}). A simple model for number up in rectangular panels is given in [14].

Applications usually contain multiple values of resistors to be embedded. Resistor yields are computed separately for each value of resistor (see subsection B), however, various valued resistors are not differentiated in the calculation of trim or rework times, or the layer pair fabrication costs, since these quantities are assumed to be averaged over a large quantity of layer pairs.

A. Cost Models for Trimming and Rework

Cost models were developed for both the trimming and rework processes. The models included capital, labor, sustainment, and performance costs. For trimming it was assumed that a laser trimming machine was purchased, and in the case of rework, the process was assumed to be a mix of manual reworking and jet printing (requiring the purchase of a jet printer). Table II shows the assumed inputs for the processes.

TABLE II – SIGNIFICANT COST MODEL INPUTS

	Laser Trimming	Automated rework (ink-jet printing)	Manual rework
Capital cost of equipment or process	$475,000	$250,000	$20,000
Residual sale value of equipment	$100,000	$50,000	$0
Operator utilization	0.2	0.5	Computed after (3)
Operator labor rate ($/hour)	$20	$20	$15
Labor burden multiplier	2.0	2.0	2.0
Scheduled maintenance costs ($/year)	$25,000	$12,000	$0
Change over time (min/design)	30	15	4
Change overs per week	10	5	5
Setup time (load + unload) per layer pair instance (min/panel)	0.33	2	0.4
Time to rework one resistor (min), T_r	NA	0.8	1.5
Utility consumption (kW)	3	0.72	0.1
Material consumption ($/resistor)	NA	0.0045	0.01
Fraction of rework attempts resulting in repariable defects	NA	0.05	0.07
Fraction of rework attempts resulting in non-repariable defects	NA	0.01	0.015

Cost of ownership models (see Appendix A) were used to compute the average trimming and rework cost per embedded resistor layer pair. We have assumed that the trimming and rework equipment is fully utilized, i.e., if it is not performing trimming or rework on the current product, it is performing it on some other product.

Note, the cost of ownership model appropriately accounts for the cost of the layer pairs with unrepairable defects introduced by trimming and rework, however, the probability that some resistors have values below their

respective L is not specifically accounted for in the cost of ownership model. To account for this, the yield of the portion of an embedded resistor layer pair associated with one board is given by,

$$Y_b = \prod_{i=1}^{a} Y_i^{N_{bi}} \quad . \tag{5}$$

where

Y_i = the post trim and rework (rework above HSL) yield of the ith resistor value on a single board,

$Y_{\text{post trim + rework + rework above HSL}}$ (which is the area under the distribution in Fig. 1b above L).

N_{bi} = quantity of the ith resistor value on a single board

a = number of different resistor values embedded in a single board.

Since (5) is the yield of a one board portion of a layer pair (not the layer pair yield), in order to properly account for it in the final cost metric we must divide the cost per layer pair by the number up. The final metric for comparison that is formed is,

$$C_b = \frac{C_{rl} + C_t + C_r}{N_{up} Y_b} \quad . \tag{6}$$

where

C_b = yielded cost of a resistor layer pair per board

C_{rl} = fabrication cost per layer pair from (4)

C_t = the average trimming cost per layer pair

C_r = the average rework cost per layer pair

N_{up} = number of boards per panel (number up).

Equation (6) is only a metric for comparison purposes that will allow an apples-to-apples comparison to be made. Note, the implicit assumption in (6) is that the processing of every layer pair (whether all the boards on it are "good" or not) is completed. The analysis in this paper only considers the process through the conclusion of layer pair processing and makes no assumptions about how or when the layer pairs are used in the fabrication of the multilayer board.

B. Modeling Resistor Quantity and Fabrication Yield

The cost model requires a calculation of the number of resistors that have to be trimmed and reworked, and the yield of the layer pairs after trimming and reworking. In order to obtain these quantities, we first must compute the resistance values of the various points on Fig. 1b. The low and high specification limits are given by,

$$\mathrm{LSL} = \mathrm{R_a}\left(1 - \mathrm{t}\right), \tag{7}$$

$$\mathrm{HSL} = \mathrm{R_a}\left(1 + \mathrm{t}\right), \tag{8}$$

where LSL and HSL have units of ohms, t is the design tolerance for the resistor (as a fraction) and R_a is the application target resistance. The fabrication target resistance, R_f is given by,

Centered Process: $$\mathrm{R_f} = \mathrm{R_a}, \tag{9a}$$

Maximizing Area Between LSL and L: $$\mathrm{R_f} = \frac{\mathrm{R_a}\left(1 - \mathrm{t} + \mathrm{L}\right)}{2}, \tag{9b}$$

where L is the lowest trimmable resistor, $L=0.55R_a$ (assumed to be 55% of the application target value for the resistor in this study). In actuality, maximizing the area between HSL and L maximizes the number of usable resistors, however, the area between LSL and L is maximized because it is difficult to accurately target HSL-L for a relatively small decrease in processing effort. In addition, all the resistors need to be probed and measured before trimming, and actually performing trimming has less impact on the trimming process throughput. Thus, for practical purposes, it is better to maximize the number of resistors with a pre-trimming value between LSL and L.

Next, we need to determine the standard deviation of the resistor values as fabricated. This defines the resistance distribution and allows computation of the yield of the resistor before and after trimming and rework. The resistor could vary in width, length (the length variation is due to variations in the distance between the contacts), thickness, or material properties. These variations are possible whether the resistor is fabricated using an additive or subtractive process. Figure 4 shows the interpretation of length and width variations (see Appendix B for an embedded resistor tolerance analysis).

Variation in the effective material resistivity, $R_{\square}$ (ohms per square), is caused by a combination of thickness and material uniformity variations; we have chosen to represent all this variation using a single parameter σ_t (the standard deviation of the thickness). We also assume that the thickness variation represents the variation from one resistor to another (not the variation within a single resistor).

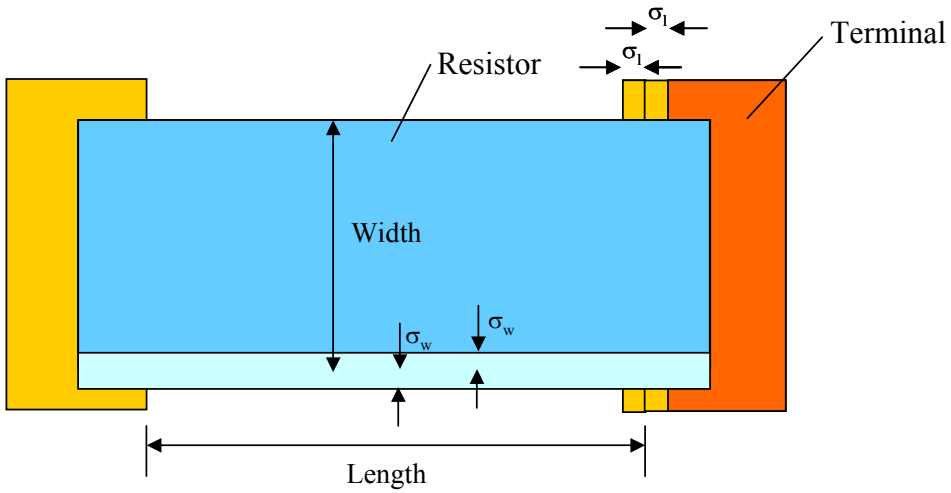

Fig. 4 – Variations in embedded resistor length and width.

In order to determine the standard deviation in the fabricated resistance value, a simple Monte Carlo analysis on the following calculation of resistor value is used,

$$R = R_{\square} \frac{T_{mean}}{T} \frac{L}{W}. \tag{10}$$

Normal distributions for the L, W, and T (the length, width, and thickness) of the resistor were assumed based on the T, L, W, σ_t, σ_l and σ_w associated with the particular resistor of interest. Note, we need not treat variations in $R_{\square}$ and T separately, one or the other will do. 5,000,000 samples were run for each resistor to obtain distributions of the resistance values, from which a standard deviation in the fabricated resistance (σ_R) value could be obtained (an example distribution generated using the Monte Carlo analysis is shown in Fig. 5).

Knowing the standard deviation in resistance value, we can evaluate various resistor yields that result from the resistor fabrication process. The yield of fabricated resistors can be inferred from Fig. 1b:

$Y_{no\ trim}$ = area under the distribution in Fig. 1b between HSL and LSL

$Y_{post\ trim + rework}$ = area under the distribution in Fig. 1b between HSL and L

$Y_{post\ trim + rework + rework\ above\ HSL}$ = area under the distribution in Fig. 1b above L

$Y_{centered\ with\ no\ trim}$ = area under the distribution between HSL and LSL where R_a is the most likely value in the distribution.

From the yields, we need to determine the number of resistors that require trimming and reworking:

Number of resistors requiring trimming/panel:

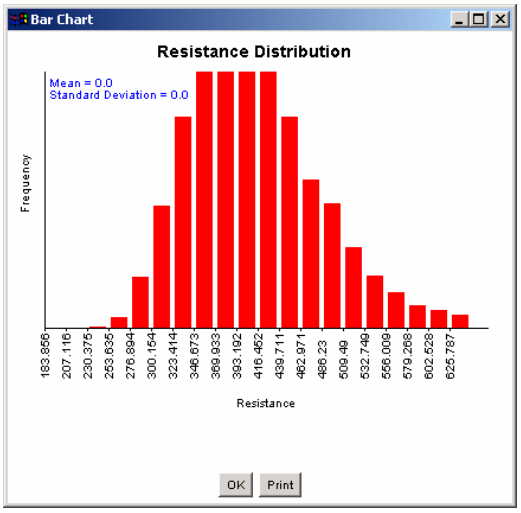

Fig. 5 – 20 mil x 40 mil resistor, 1 mil standard deviation on width and length, 0.2 mil thick, 0.03 mil standard deviation on thickness (15%), $R_{\square}$ = 200 ohms/square. The standard deviations assumed for this example may be unrealistically large for actual embedded resistors, but were chosen so that the distribution's skew to the right (similar to Fig. 1a) would be obvious.

$$N_t = N_b N_{up}(\text{area under the distribution in Fig. 1b between LSL and L}), \tag{11}$$

Number of resistors above HSL/panel:

$$N_{r1} = N_b N_{up}(\text{area under the distribution in Fig. 1b above HSL}), \tag{12}$$

where

N_b = number of resistors on a board $= \sum_{i=1}^{a} N_{b_i}$

N_{up} = number of boards per panel.

The number of resistors that require rework due to trimming errors is,

$$N_{r2} = N_t Y_{trim}, \tag{13}$$

where Y_{trim} is the yield of the trimming process.

IV. Results

The model discussed in Section III has been used to assess the three different applications described in Table III.

TABLE III – EXAMPLE APPLICATIONS CONSIDERED IN THIS ANALYSIS, ONLY EMBEDDABLE RESISTORS ARE SHOWN

Embedded Resistor Value (ohms)	**Fiber Channel Card (12 x 18 inch) Quantity per board**	**Picocell Board (2.27 x 6.87 inch) Quantity per board**	**High-Density Picocell Board (2.17 x 2.17 inch) Quantity per board**
100	210	27	27
500	181	19	19
5000	150	22	22
50000	63	1	1
100000	6	1	1

The first step in the analysis is to generate the relationship between the size of a standard deviation in the printing, plating or etching process and cost. For simplicity we assume that the size of one standard deviation in the printing, plating or etching process is the same in both planar directions. We represent cost as the cost of a resistor layer pair (i.e., a layer pair with embedded resistors fabricated in it) per board, or the cost of an embedded resistor layer pair divided by the number of boards fabricated per panel. The "per board" is necessary to appropriately accommodate the board (resistor) yield as discussed in Section II.

Figure 6 shows a result for the Fiber Channel Card example case where all the embedded resistors are subject to a 0.1% or a 10% design tolerance. Several different scenarios are considered in Fig. 6. In Fig. 6a, trimming without rework is the most economical approach when one printing, plating or etching standard deviation is less than 2.1 mils, whereas above 2.1 mils, it becomes economical to trim and perform rework (including reworking resistors above the HSL). If rework is to be performed, it is always preferable to rework the resistors above the HSL; also we

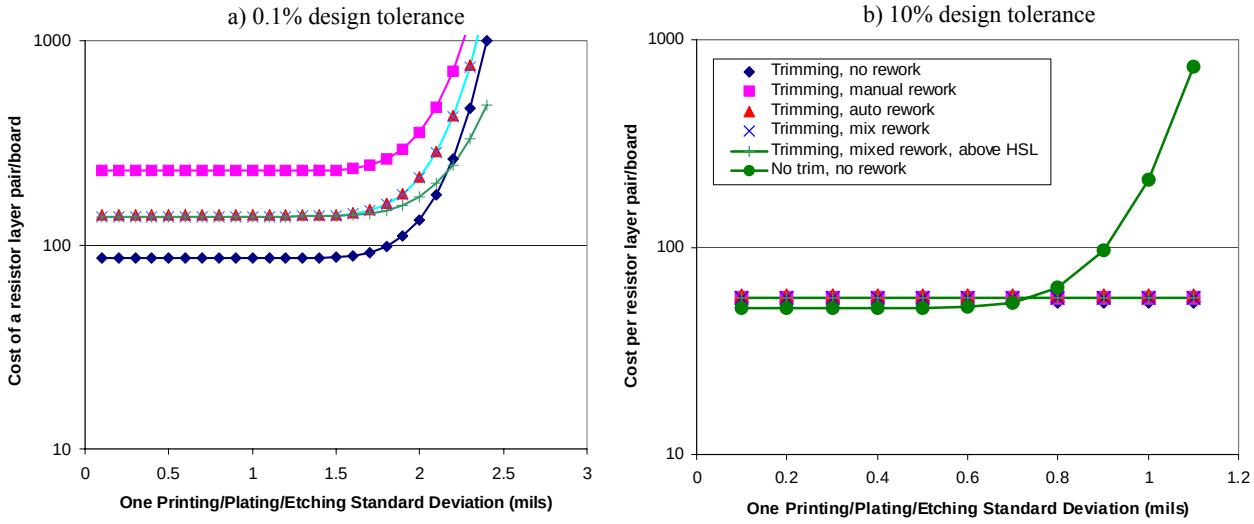

Fig. 6 – Cost of resistor layer pairs for the fiber channel card with various design tolerances on embedded resistors.

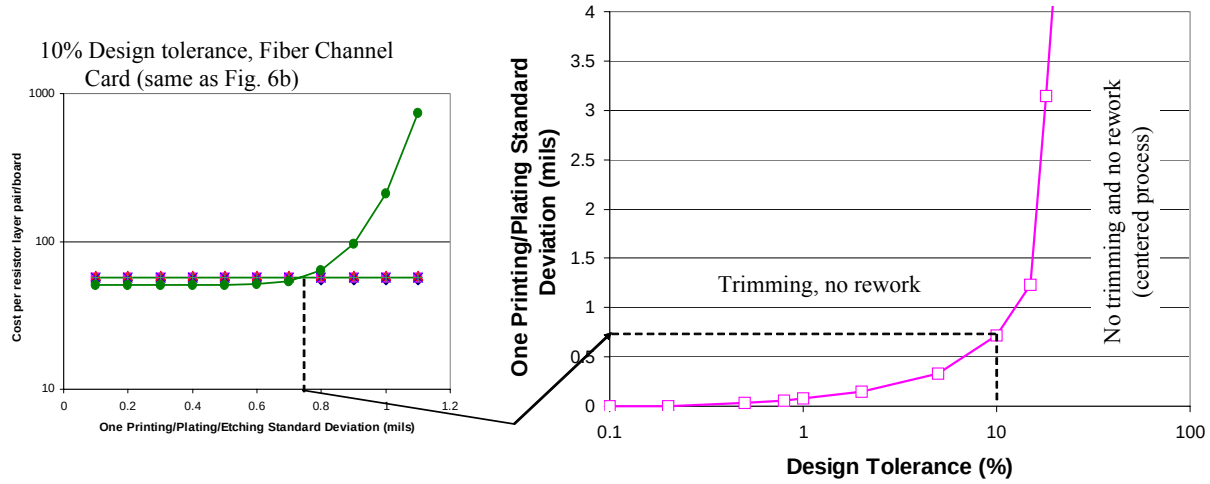

Fig. 7 – Determining the regions of applicability of trim and rework by plotting the intersection points between the various trim and rework scenarios. See Fig. 6b for definition of the points in the left plot.

find that a mixed manual and automatic rework process[1] is always as good or better than just performing manual or just automatic rework. In Fig. 6b, for a larger design tolerance, the no trimming solution is the most economical when one printing or plating standard deviation is less than 0.73 mils. Above 0.73 mils any other solution that involves trimming is preferable. Note, for this example there are very few resistors above HSL and very few resistors ever require any sort of rework, so all the solutions are virtually identical.

In order to create a more general result, we wish to extract just the points where the various trim and rework scenarios intersect in Fig. 6. As an example, consider Fig. 7. In Fig. 7, we have varied the design tolerance on the resistors in the fiber channel card (same design tolerance assumed for all resistors in the application) and plotted the intersection between the *no trim, no rework* solution and the *trim, no rework* solution (the 10% design tolerance solution, that intersects at σ = 0.73 mils is shown as an example in Fig. 7). Using this process, the boundary between not performing any trimming or rework (with a centered process) and a trimming solution with no rework for the fiber channel card example is generated. Performing this process on all three examples given in Table III and also including the intersection between the *trim, no rework* and *trim and rework* solutions we obtain the result in Fig. 8. Figure 8 shows that for three very different applications (widely different board sizes and numbers of embedded resistors), the regions of applicability of trimming and rework are surprisingly well defined. For the three

[1] The mixed rework solution uses a manual process (see Table II for details) until 50% or more utilization of an automatic ink-jet printer is attained. The first automatic ink-jet printer is supplemented with manual rework until 50% or more utilization of a second ink-jet printer is attained, etc.

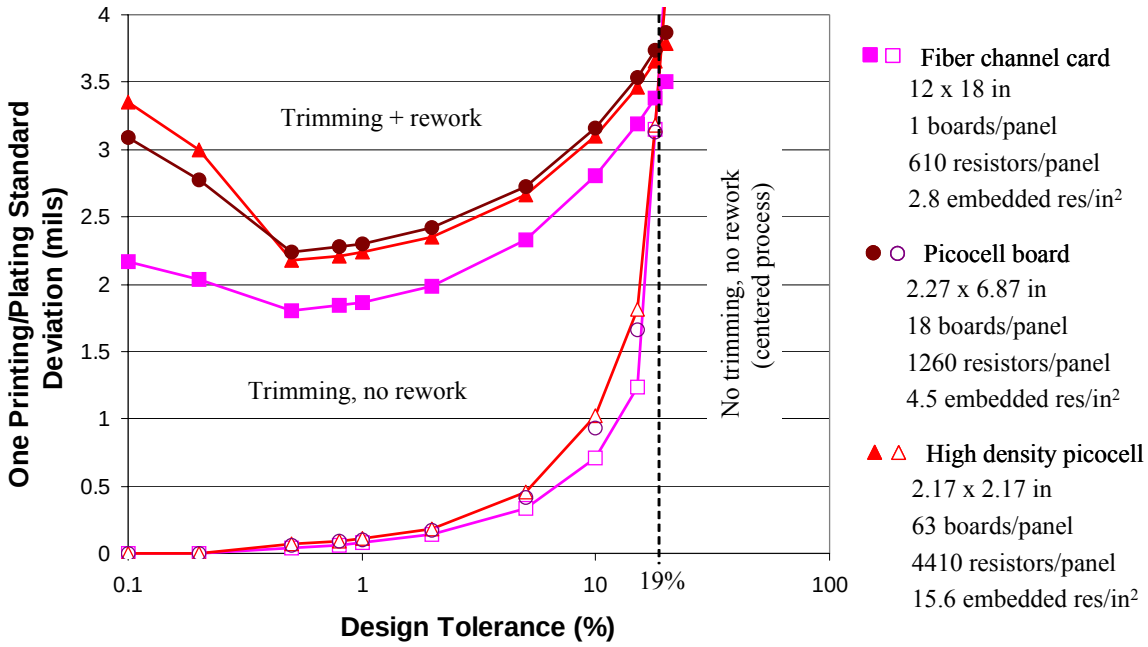

Fig. 8 – General trimming and rework relationship (no thickness variation in fabricated embedded resistors).

applications considered, if the design tolerance on the resistors is greater than 19%, the resistor fabrication process should be centered and no trimming or rework performed. The boundary between performing rework and not performing rework tends to rise as the design tolerance drops below 0.5%, because the investment in the rework process escalates quickly once the design tolerance is below 0.5% (above 0.5% there are very few resistors that need to be reworked and the rework investment is small).

So far the result shown in this section have not addressed variations in the embedded resistor thickness (Fig. 8 is for an assumption of no variation in the resistor thickness). As thickness variation grows, the boundaries shown in Fig. 8 shift down, as shown in Fig. 9.

Due to the assumption that the trimming and rework equipment is fully utilized and depreciated over 5 years, there is relatively little sensitivity in the model to the equipment cost. Changing the cost of the trimming process (i.e., changing the trimming equipment cost) shifts the boundary between the *trim, no rework* and *no trim or rework* left to right. If the trimming equipment cost is decreased the boundary shifts to the right, if it is increased it shifts to the left. However, this boundary is not very sensitive to the trimming equipment cost. Changing the rework characteristics (i.e., changing the length of time required by the automatic rework equipment to rework a resistor), changes the left side of the boundary between *trim and rework* and *trim, no rework*, Fig. 10.

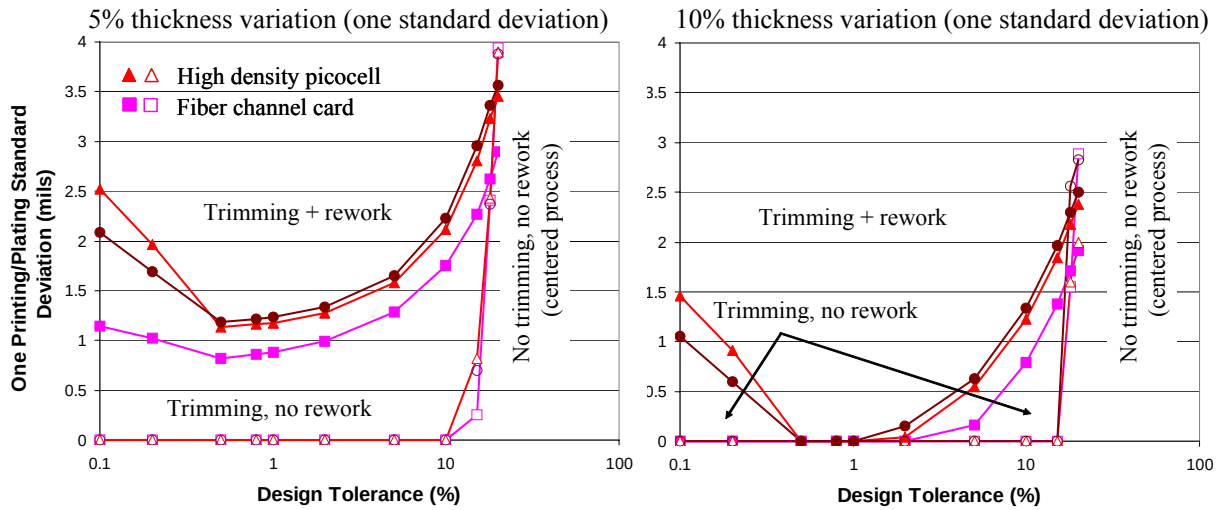

Fig. 9 - General trimming and rework relationship including thickness variations.

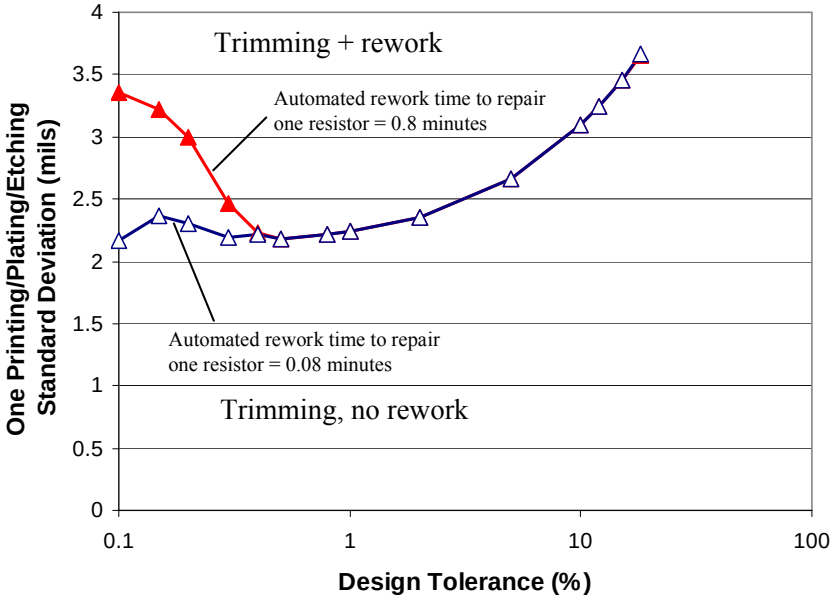

Fig. 10 – Variation in the automatic rework equipment throughput for the high-density picocell application with no thickness variation.

The left side of the relation shown in Fig. 8, and the boundary between reworking and not reworking trimmed resistors is sensitive to the yield of the trimming process. When C_{pk} decreases, causing the trimming yield to decrease as shown in Fig. 2, two competing effects take over for low design tolerances: 1) for trimming with no rework, the cost of trimming is unchanged but the yield of the resulting boards drops (causing an increase in the yielded cost); 2) for trimming with rework, the yield of the resulting boards is approximately unchanged, but their cost increases because there is more rework (also causing an increase in yielded cost). The lines in Fig. 11 are not

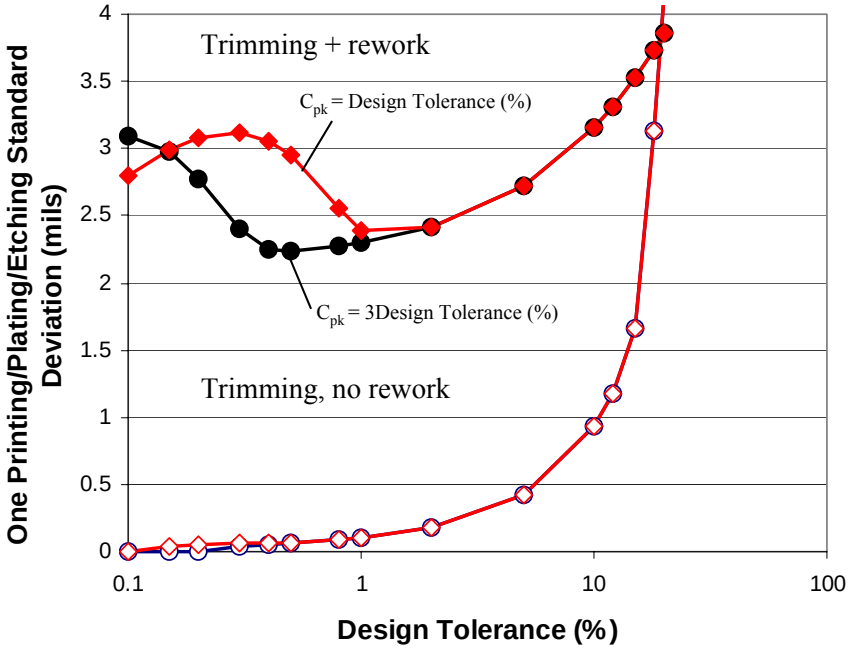

Fig. 11 – Variation in the general trimming and rework relationship with trimming yield (no thickness variation in fabricated embedded resistors) for the Picocell Board.

showing yielded cost (obviously as trimming yield decreases, yielded costs increase for all cases), rather, they show whether the relative contributions of the cost of extra rework decreasing yield, which contribute at differing rates as design tolerance decreases. For large design tolerances, the trimming yield is very close to 100% for all C_{pk} assumptions and therefore, the results are unaffected.

The asymptotic approach to the 19% design tolerance demonstrated in Figs. 8-11 is most sensitive to the lowest trimmable resistor (L) value. In Fig. 12a, L is varied and the boundary between *no trimming* and *trimming, no rework* is plotted. Plotting the points at which the boundary crosses the 3 mil printing/plating/etching standard deviation (approximately the asymptote), we obtain Fig. 12b. While Fig. 12a is dependent on the thickness variation (result for 0% thickness variation is shown), Fig. 12b is found to be independent of the thickness variation and have the functional form shown on the figure. The result in Fig. 12b suggests the following: when,

$$t > -0.317L + 35.05 \tag{14}$$

the resistor fabrication process should be centered and no trimming should be done, where t is the design tolerance on the resistors (in %) and L is the lowest trimmable resistor as a % of the application target resistance. Note, as demonstrated in Fig. 9, (14) is more accurate as the variation in the thickness (or material properties) of the embedded resistor increases. At low values of thickness (material property) variation and small standard deviation

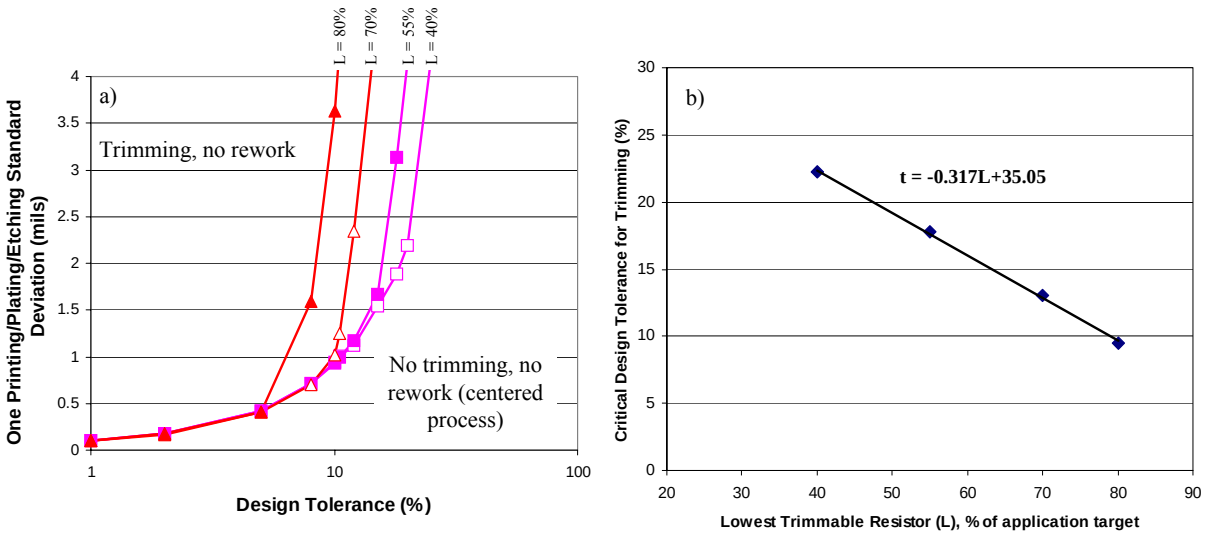

Fig. 12 – a) Variation in the boundary between trimming and no trimming with lowest trimmable resistor value (L) for no thickness variation in the Picocell Board application. L is the % of the application target resistance. b) Plot of design tolerance at which boundaries from a) cross the 3 mil standard deviation in printing, plating or etching.

in the length and widths, the no trimming region can be extended to considerably tighter design tolerances. For (14) to be used as a design guideline, its sensitivity to parameter variations needs to be explored in more detail than what is included in this paper.

V. Discussion and Conclusions

The results presented in this paper, although application-specific, clearly define regions where trimming, rework and no trimming or rework are economically advantageous. The boundary between not trimming and trimming (with no rework) is also well defined, i.e., application unspecific. We find that when $t > -0.317L + 35.05$, trimming and rework of embedded resistors does not make sense for any level of variation in the fabrication process or material properties. The boundary between trimming with and without rework is application independent when design tolerances are larger than ~1%, where relatively few resistors require reworking, but for tighter design tolerances, significant investments in the rework process become necessary and the boundary is very sensitive to the application properties and the rework equipment cost.

The model developed in this paper is targeted at the system design and planning phases as part of the cost-benefit analysis used to determine the application-specific value of embedding passive components; and more specifically the particular mix of passive components to embed. The model proposed in this paper allows a system

designer to determine whether embedding particular resistors is going to require trimming and/or rework so that the associated costs of these activities can be assessed as embedded content decisions are made.

There are several effects that could be modeled in more detail to improve the accuracy of the results in this paper. We have assumed the same design tolerance on all resistors in the application; in reality some resistors will have tight tolerances and others can be allowed considerably larger variation depending on their functional role in the circuit. It also should be pointed out that this paper makes the assumption that the manufactured resistors are independently identically distributed, whereas in reality, the physical processes that may cause a distribution of resistance values may be strongly correlated from board to board (or batch to batch). We have also approximated the distribution of fabricated resistors as a normal distribution, when in actuality it tends to skew slightly toward higher values (Fig. 1a).

APPENDIX A – COST OF OWNERSHIP (COO) MODELS

Historically, purchase decisions for equipment have been based on initial purchase and installation costs. However, purchase costs do not consider the effect of equipment reliability, utilization, and yield. Over the life of the system, these factors may have a greater impact on cost-of-ownership than initial purchase costs. Lifetime cost-of-ownership per good product is generally sensitive to production throughput rates, overall process reliability, and yield, and it is relatively insensitive to initial equipment purchase price. While initial COO models were developed for wafer fabrication equipment [15], COO can easily be extended to other applications, [16].

The basic cost-of-ownership algorithm is described by,

$$C_{ownership} = \frac{C_{fixed} + C_{variable} + C_{yield\ loss}}{(TPT)YU}, \tag{A.1}$$

where:

C_{fixed} = Fixed cost – purchase, installation, etc.

$C_{variable}$ = Variable cost – labor, material, utilities, overhead, etc.

$C_{yield\ loss}$ = Cost due to yield loss – money invested into scrapped parts and production lost by producing defective parts

TPT = Throughput

Y = Composite Yield

U = Utilization – ratio of production time to total available time.

For the purposes of this study, COO contributions from capital, sustainment, and performance are considered. The miscellaneous inputs needed by the COO model (in addition to those in Table I) are given in Table A.I.

TABLE A.I – COO MODELING ASSUMPTIONS

Production hours per week	160
Production weeks per year	50
Labor rate for maintenance and change overs	$20/hour
Labor burden	2.0
Profit margin on finished embedded passive boards	15%
Depreciation life of equipment	5 years
Conventional layer pair cost	$12.50/ft^2
Extra embedded resistor processing cost	$7.43/layer pair*
Extra embedded resistor processing cost	$0.01/embedded resistor
Energy cost	$0.08/kWh
Cost of repairing a defect caused by the rework process	$20/resistor

*An additive embedded resistor process is assumed.

All of the costs are computed using versions of the general form in (A.I). Capital costs treat the costs to buy the machine, facilities, and/or process, how it depreciates, and what value it has at the end of the depreciation period. Sustainment treats all the costs required to keep the machine, facility and/or process operational. Both scheduled and unscheduled maintenance contribute to sustainment cost. Labor content, replacement parts and other materials are included. In some cases all the maintenance costs may be subsumed by maintenance contracts, the cost of which may be substituted for the scheduled and/or unscheduled maintenance costs. Performance costs measure the value (or lack thereof) of having the machine, facility or process included by treating change-overs, repairable and non-repairable defects and cycle time. Also contributing to performance costs are repairable and non-repairable defects introduced by the machine, facility and/or process.

APPENDIX B – TOLERANCE ANALYSIS FOR EMBEDDED RESISTORS

The largest increase and decrease in resistance value that could result from a one standard deviation variation in the resistor geometry shown in Fig. 4 is given by,

Largest Increase: $$\Delta R_{f\uparrow} = R_{f_{actual}} - R_{f_{design}} = \frac{R_{\square}\left(\frac{l_{design} + \sigma_l}{w_{design} - \sigma_w}\right)t_{design}}{t_{design} - \sigma_t} - R_{\square}\left(\frac{l_{design}}{w_{design}}\right), \quad \text{(B.1)}$$

Largest Decrease: $$\Delta R_{f\downarrow} = R_{f_{design}} - R_{f_{actual}} = R_{\square}\left(\frac{l_{design}}{w_{design}}\right) - \frac{R_{\square}\left(\frac{l_{design} - \sigma_l}{w_{design} + \sigma_w}\right)t_{design}}{t_{design} + \sigma_t}, \quad \text{(B.2)}$$

where

$$R_{f_{design}} = R_{\square}\left(\frac{l_{design}}{w_{design}}\right),$$

$R_{\square}$ = the resistivity of the embedded resistor material (ohms/square),

l_{design}, w_{design} and t_{design} = the designed length, width, and thickness of the embedded resistor,

σ_l, σ_w and σ_t = magnitude of one standard deviation in the length, width and thickness of the embedded resistor.

Equations (B.1) and (B.2) provide the full range of possible resistance values that can result from a one standard deviation variation in the length, width and/or thickness of the embedded resistor. Similar tolerance analysis models for embedded resistors appears in [17] and [18].

One could estimate the variation in fabricated resistor values by averaging $\Delta R_{f\uparrow}$ and $\Delta R_{f\downarrow}$ from (B.1) and (B.2). This estimate of variation is, however, conservative, i.e., it will predict a variation that is greater than (or equal to) the standard deviation obtained via the Monte Carlo analysis. Estimating the standard deviation in this way was found to be accurate only for resistors with values greater than ~2000 ohms. For smaller values of resistance, the estimated standard deviation could be as much 2 to 3 times larger than the standard deviation obtained via the Monte Carlo analysis.

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