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13. The Economics of Embedded Passives

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13.1 Introduction

In the past, engineers involved in the design of electronic systems did not concern themselves with the cost effectiveness of their design decisions; that was someone else's job. Today the world is different. Every engineer in the design process for an electronic product is also tasked with understanding the economic tradeoffs associated with their decisions. Nowhere is the need for economic analysis more critical than when emerging technologies, materials, and processes are involved, for it is the decisions of if, when and where to insert new technologies that often separates the winners from the losers in high-tech products.

Economics encompasses an assessment of the total life cycle cost of a design decision where the life cycle includes the design, manufacturing, testing, marketing, sustainment, and end-of-life of the product. The decision to convert discrete passives to embedded passives is much further reaching than simply reducing the cost of part procurement and paying more for the board. There are a host of other cost and benefit issues to be considered that translate into life cycle economics at some level. In this chapter we attempt to touch on the economic attributes of a system's design, production, and support that impact the decision to use embedded passives.

Embedded passives are fabricated within substrates and, while embedded passives will never replace all passive components, they provide potential advantages for many applications. The generally expected advantages include:

- Increased circuit density through saving real-estate on the substrate
- Decreased product weight
- Improved electrical properties through additional termination and filtering opportunities, and shortening electrical connections
- Cost reduction through increasing manufacturing automation
- Increased product quality through the elimination of incorrectly attached devices
- Improved reliability through the elimination of solder joints.

Potentially the biggest single question about embedded passives is their cost, "…of all the inhibitors to achieving an acceptable market for integral substrates, the demonstration of cost savings is paramount" [1]. There is considerable controversy,

however, as to whether applications fabricated using embedded passives will be able to compete economically with discrete passive technology. On the bright side, the use of embedded passives reduces assembly costs, shrinks the required board size, and negates the cost of purchasing and handling discrete passive components. However, these economic advantages must be traded off against the higher cost (per unit area) of boards fabricated with embedded passives (a situation that will not disappear over time) and possible decreases in throughput of the board fabrication process.

Several different cost estimates for embedded passives have been presented. These estimates range from embedding resistors in a digital application resulting in a 73% savings [2] and embedding inductors and capacitors in a RF application resulting in a 27% savings [2], the cost per square inch of embedded resistor ranging from $0.15 to $0.30 from 6 x 6 inch to 24 X 24 inch substrates, [3], and combined 80% improvement in cost/size figures of merit for MCM-D/embedded passives over a surface mount on PCB solution for a GPS receiver front end, [4]. All these estimates, while not necessarily inaccurate, are also obviously application-specific and of limited use in decision making for an unrelated application. Understanding the true economic impact of introducing embedded passives can not be captured in a single simple number, and tradeoff decisions should not be made based on such simplified metrics.

The application-specific costs depend on many effects when embedded passives are present in a board:

- Decreased board area due to a reduction in the number of discrete passive components
- Decreased wiring density requirements due to the integration of resistors and bypass capacitors into the board
- Increased wiring density requirements due to the decreased size of the board
- Increased number of boards fabricated on a panel due to decreased board size
- Increased board cost per unit area
- Decreased board yield
- Decreased board fabrication throughput
- Decreased assembly costs
- Increased overall assembly yield
- Decreased assembly-level rework.

Several other recurring system costs may also be affected by the use of embedded passives, for example: the need to electromagnetically shield the board may be reduced or eliminated when certain passives are embedded (saving on expensive materials and their assembly), and the costs associated with thermal management of the board may all be affected.

Due to the opposing nature of many of the effects listed above, the overall economic impact of replacing discrete passives with embedded passives is not trivial to determine and, in general, yields application-specific guidelines instead of general rules of thumb. In fact the very nature of tradeoff analysis is one in which *the greater the detail*

necessary to accurately model a system, the less general and more application-specific the result.

13.2 Modeling Embedded Passive Economics

Several authors have addressed cost analysis for embedded passives and thus provide varying degrees of insight into the economic impact of embedded passives. The target of all these economic analyses is to determine the effective cost of converting selected discrete passive components to embedded components. The most common approach to economic analysis of embedded passives is to: 1) reduce the system cost by the purchase price and conversion costs[1] associated with the replaced discrete passives, 2) reduce the board size by the sum of the layout areas associated with the replaced discrete passives and determine the new number of boards on the panel, and 3) determine the new board cost based on a higher per unit area cost for the embedded passive panel fabrication and the new number-up computed in step 2. The results of these three steps determine the new system cost. The effects included in this first-order approach are critical, however, the approach ignores several additional elements, most notably: decreased throughput for embedded passive board fabrication means that board fabricators will have to apply higher profit margins for embedded passive boards to justify their production on lines that could otherwise be producing conventional boards; routing analysis of the board to determine not only what layers may be omitted, but what layers may have to be added to maintain sufficient wiring capacity as passives are integrated and the board is allowed to shrink; yield of both discrete passive components and the variation in board yield due to embedding passives; and potential reductions in rework costs (due to both assembly defects and intrinsic functional defects) associated with discrete passives.

Brown [2] presents an outline of all the potential contributions to the life cycle cost of embedded passives. Rector [1] provided the economic analysis that appeared in the 1998 NEMI Passive Component Technology roadmap [5] using the first-order approach outlined above. Rector concludes that embedded passives can be economically feasible, but only if one considers more than the effects in the first-order model outlined above, but does not provide a quantitative analysis to support this supposition. Ohmega Technologies Inc. has also generated a cost model for assessing cost tradeoffs associated with its Ohmega-Ply® embedded resistor material, [6]. The Ohmega cost model follows the first-order approach described above, and includes yield and rework effects. Ohmega concludes that 2-4 embeddable resistors per square inch are required to make the use of the Ohmega-Ply material economically practical.

Realff and Power developed a technical cost model for board fabrication and assembly [7]. The model includes test (board and assembly), yield, and rework. The focus of the model is on the equipment requirements, under the assumption that embedded resistors are fabricated using a dedicated resistor layer, they conclude that for

[1] Conversion costs are the handling, storage and assembly costs associated with a discrete component.

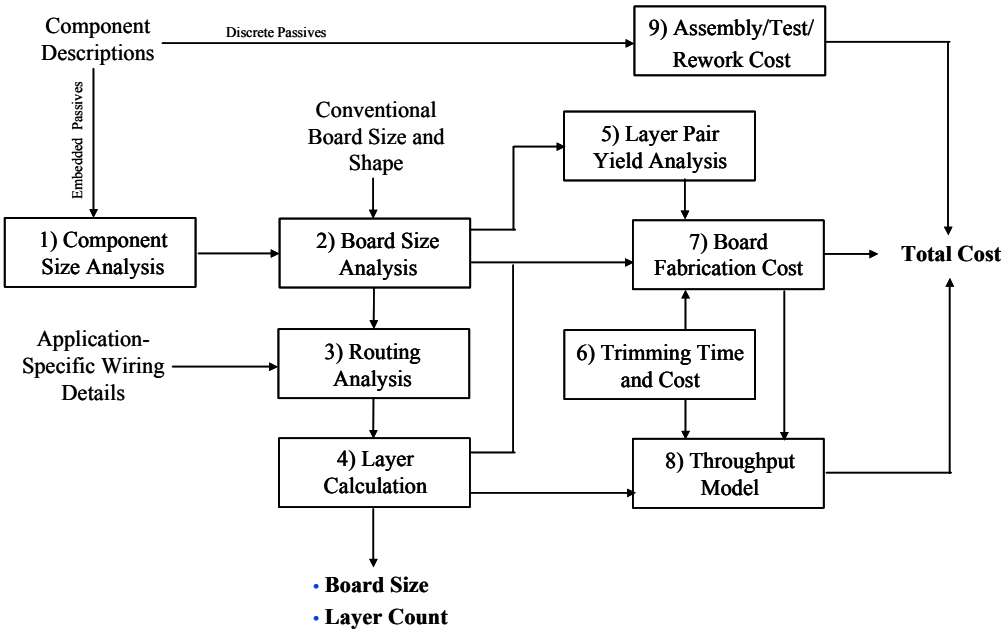

Figure 1 – Embedded passive board cost tradeoff model [10].

embedded resistors to have a significant impact on the cost of a system, their use must allow the removal of equipment or in some other way fundamentally change the assembly process (e.g., changing from double to single sided assembly). Power *et al.* [8] extend the model in [7] to embedded capacitors and cast it in the form of an optimization problem targeted at choosing which discrete passives to integrate based on an assumption of assembly and substrate manufacturing process details, and material properties.

Another analysis that recently appeared focused on design tradeoffs for a GPS front end, [4]. This analysis includes detailed cost modeling of thin-film embedded resistors and capacitors performed using the Modular Optimization Environment software tool from ETH, [9].

A recent manufacturing cost model from Sandborn *et al* [10], incorporates quantitative routing estimation and assesses board fabrication throughput impacts for setting profit margins on board fabrication, effects that have not been included in previous models. This model is outlined in Figure 1.

Qualitatively the model in Figure 1 works in the following way:

1. Accumulate the area of the footprints of discrete passives to be embedded.
2. Reduce board area by the accumulated discrete passive area from step 1 maintaining the aspect ratio of the original board. This step is optional, i.e., the board area may be fixed.
3. Plated or Printed Resistors: Determine the area occupied by each plated or printed embedded resistor on wiring layers. Perform routing analysis removing

nets and vias associated with resistors that are embedded and accounting for area blocked by embedded resistors on wiring layers. Routing is assumed to be unaffected by discrete resistors embedded using Ohmega-Ply® or similar dedicated layer addition approaches. Bypass Capacitors (distributed capacitors): All nets and vias associated with embedded bypass capacitors are removed from the routing problem. Singulated Capacitors: Assume that embedded singulated capacitors do not affect routing analysis. Using these assumptions determine the relative change in routing resources due to embedding selected passives.

4. Using the layer requirements, the relative routing requirements for the embedded substrate and either a fixed measure of the routing efficiency associated with the conventional board or a range of possible efficiencies determined under the assumption that the conventional version of the board did not include any more layer pairs than it needed to route the problem, compute the number of required layer pairs for the embedded passive implementation.
5. Determine the yield of layer pairs that include embedded passives.
6. Determine the trimming cost for embedded resistors. The necessity of trimming is determined by the resistor's tolerance. The application-specific cost per trim is determined by modeling the throughput of a laser trimming process.
7. Compute the number of boards per panel from the board size (number-up) and the effective panel fabrication costs from the layer and material requirements, yields, and resistor trimming costs.
8. Determine the relative board fabrication profit margin from layer pair throughput modeling (see discussion in Section 13.3).
9. Accumulate assembly cost, test, rework, and board fabrication costs (with profit margin) to obtain total relative cost. The analysis in Figure 1 focuses on differences in system cost between embedded passive and discrete passive solutions, therefore all cost elements that are approximately equivalent for the embedded and conventional system are igonored, e.g., all functional testing of the system and, procurrement and assembly costs associated with non-embeddable parts.

13.3 Key Aspects of Modeling Embedded Passive Costs

In this section several of the key aspects that are necessary for the assessment of embedded passive costs are discussed in detail by providing tradeoff level analyses. Note the following focuses on embedded resistors and capacitors; however, the concepts are generally applicable to inductors as well.

13.3.1 Board Size and Routing Calculations

Board size is critical to the cost analysis because it determines the number of boards that can be fabricated on a panel (number up) and is a key input to the determination of the number of required layers for wiring. As discrete passive components are converted to embedded passives, the physical size of the board can either remain fixed or be allowed to decrease by the layout area associated with the discrete passives given by,

$$A_{new} = A_{conv} - \sum_{i=1}^{N} (l_i + S)(w_i + S) \quad (1)$$

where S is the minimum assembly spacing, l_i and w_i are the length and width of the ith discrete passive, N is over all discrete passives that are converted to embedded passives, and A_{conv} is the conventional board area. If the board is double sided, the calculation in (1) can be performed independently for each side of the board, the larger of the two sides determines the new board size.

The area consumed by the embedded passives fabricated directly on internal wiring layers impacts the tradeoff analysis by decreasing the wiring available on internal layers. Embedded resistors that are fabricated using a dedicated layer pair, e.g., Omega-Ply® and Gould TCR™, do not have a first order effect on the wiring availability to the application. The area occupied by an embedded resistor on a board inner layer is given by,

$$A_R = \begin{cases} \frac{0.8R}{R_s} m^2 & \text{for } 0.8R > R_s \\ \frac{R_s}{0.8R} m^2 & \text{for } 0.8R \le R_s \end{cases} \quad (2)$$

where R is the value of the resistor (Ω), R_s is the sheet resistivity of the resistor material (Ω/square), and m is the minimum feature size for embedded resistor fabrication. Since embedded resistors are designed and fabricated to smaller (resistance) values than required and trimmed, a factor of 0.8 is included in (2).[2]

There are two types of capacitors that must be considered - bypass (decoupling) capacitors, and singulated or non-bypass capacitors. We assume that bypass capacitors can be absorbed into dedicated bypass layer pairs (planar distributed capacitance layers) and the non-bypass capacitors must be fabricated individually on a dedicated capacitor layer pair if they are to be embedded. The area occupied by an individual non-bypass embedded capacitor on a capacitor layer pair is,

$$A_C = \frac{C}{c} \quad (3)$$

where C is the value of the capacitor, and c is the capacitance per unit area of the capacitor layer pair. Assuming square capacitors, the number of embedded capacitor layer pairs (for non-bypass capacitors) required in the board is given by,

[2] The factor of 0.8 can be derived assuming a symmetric distribution of fabricated resistor values where the lowest trimmable resistor is 55% of the application target value, a 5% design tolerance on the resistors, and maximizing the number of resistors between the high specification limit and the lowest trimmable resistor, see Figure 3 in Section 13.3.4.

$$N_{\text{integral cap layers}} = \left\lceil \frac{\sum_{j=1}^{N_C} \left(\sqrt{A_{C_j}} + S_c \right)^2}{A_{\text{new}}} \right\rceil \quad (4)$$

where N_C is the total number of non-bypass capacitors that are converted from discrete to individual embedded capacitors, and S_c is the effective spacing between individual embedded capacitors on the embedded capacitor layer pair. S_c is usually set larger than the minimum spacing possible to allow for perforation of the embedded capacitor layer by vias and through holes, and to allow area for interconnection.

Instead of decreasing the board area as passives are embedded, decreases in the required board surface area could be used to convert a double-sided board application to a single-sided board as discussed in [1]. This conversion would decrease assembly costs by increasing the throughput and yield of the assembly process. Whether it is realistic or even economically wise to convert a double-sided board to single sided depends on whether there is an economic advantage in allowing the board to shrink. A smaller area board only saves money only if it results in the ability to fabricate a greater number of boards per panel (note, there may be other performance or application-specific benefits to a smaller board size as well).

Besides estimating the physical size of the board after embedding of selected discrete passive components, we also need to consider the routing requirements. The following first-order routing assumptions can be made with respect to embedded passives:

- The IO (effectively the nets and vias) associated with discrete resistors that are replaced by embedded resistors that are directly fabricated on existing board inner layers are effectively removed from the routing problem, i.e., the embedded resistors are fabricated in series with the nets they are attached to on the wiring layers, however, the area occupied by the embedded resistors blocks routing and is accounted for, see (6).
- Singulated non-bypass discrete capacitors converted to embedded capacitors and embedded resistors fabricated using dedicated layer pairs have no effect on the routing problem.
- The IO (effectively the nets and vias) associated with discrete bypass capacitors converted to an embedded capacitor are effectively removed from the routing problem.

With these assumptions and the routing information from the conventional implementation, the routing requirements, and thereby the number of layers required, for an implementation that includes embedded passives can be determined. An estimation of the minimum number of layers required to route the application proceeds as follows,

$$N_{layers_{new}} = \frac{W_{used\,new} + W_{blocked}}{W_{layer\,new}} \left(\frac{U_{conv}}{U_{limit}} \right) \tag{5}$$

where U_{limit} is the maximum fraction of the theoretically available wiring in the board that can be used for routing, and U_{conv} is the fraction of that wiring that is actually used to route the conventional application. The ratio of U_{conv} and U_{limit} measures the routing efficiency of the conventional implementation. When the ratio is large (i.e., close to one), the implementation has effectively used all the wiring that is available and any additional wiring would require the addition of another layer pair or an increase in board area. At some smaller value, any decrease in wiring would allow the omission of a layer pair.

The wiring blocked ($W_{blocked}$) by embedded resistors (length of wiring that can not be used) is given by

$$W_{blocked} = \left(\frac{\sum_{i=1}^{N_R} A_{R_i}}{A_{new}} \right) \left(\frac{A_{new}}{A_{conv}} W_{layer\,conv} \right). \tag{6}$$

where N_R is the number of embedded resistors, A_{new} is give by (1) and A_R is given by (2). The second multiplier is the wiring per layer in the embedded passive board with no embedded resistors included ($W_{layer_{new}}$). The total length of wiring used for the new implementation is given by,

$$W_{used\,new} = f\left(W_{used\,conv}\right) \tag{7}$$

where f is the fractional change in required total wiring length. The wiring used in the conventional implementation is found from,

$$W_{used\,conv} = W_{avail\,conv} \tag{8}$$

where $W_{avail_{conv}}$ is the total length of wiring theoretically available in the conventional board ($W_{layer_{conv}}$ multiplied by the number of layers in the conventional board minus layers on which wiring is not done, e.g., reference planes). Assuming that the total wiring length required is proportional to the total number of system IO that require routing (a fundamental assumption in routing estimation approaches that compare requirements and resources, [11]), f is found from,

$$f = \frac{N_{IOnew}}{N_{IOconv}} \tag{9}$$

where,

$N_{IO\,new} = N_{IO\,conv} - 2N_R - 2N_{BC}$, the total number of system IO in the new implementation (assuming 2 IO per resistor and capacitor), assuming resistors are printed or plated directly onto wiring layers

N_R = number of embedded resistors

N_{BC} = number of bypass capacitors absorbed into a bypass capacitance layer pairs

$N_{IO\,conv}$ = total number of system IO in the conventional implementation.

Note, N in (1) is $N_R + N_C + N_{BC}$ where N_C is the number of non-bypass capacitors that are integrated into the board. The number of IO in the conventional implementation is given by,

$$N_{IO\,conv} = N_{nets\,conv}(\text{fanout} + 1) \tag{10}$$

where,

fanout = average number of IO that a net attaches together minus one (assumed to be the same for the conventional and embedded passives implementations)

$N_{nets\,conv}$ = number of nets in the conventional implementation.

Since layers occur in pairs in printed circuit board manufacturing, the result given by (5) is rounded up to the nearest multiple of two for use in the model. Note, the final value of $N_{layers_{new}}$ given by (5) will be independent of $W_{layer_{conv}}$.

13.3.2 Recurring Cost Analysis

Using the size and routing relationships developed in the last section, we can predict the board fabrication costs. The price per conventional board is given by,

$$P_{conv} = (1 + M_{conv})\frac{C_{layer\,pair} A_{conv} N_{layers_{conv}}}{N_{up_{conv}}} \tag{11}$$

where

M = profit margin (see Section 13.3.4)

$C_{layer\ pair}$ = cost per unit area per layer pair

$N_{up_{conv}}$ = number up, number of boards that can be fabricated on a panel

$N_{layers_{conv}}$ = total number of layers (wiring and reference) in the conventional implementation of the board.

The $N_{up_{conv}}$ is computed from the board length and width, panel length and width, minimum spacing between boards, and the edge scrap allowance using the model in [12]. The price per embedded passives board is similar to (11), with the addition of the capacitor layer costs (if embedded bypass or non-bypass capacitors are present),

$$P_{new} = \frac{(1+M_{new})}{N_{up\,new}}\left[C_{layer\,pair_{new}} Area_{new} N_{layers_{new}} + N_{bypass\,cap\,layers} C_{bypass\,cap\,layer} + N_{integral\,cap\,layers} C_{integral\,cap\,layer}\right] \quad (12)$$

where

$N_{layers_{new}}$ = minimum number of layers required to route the application given by (5)

$N_{integral\,cap\,layers}$ = number of embedded capacitor layers given by (4)

$N_{bypass\,cap\,layers}$ = number of bypass capacitor layers.

The new layer pair cost in (12) is given by,

$$C_{layer\,pair_{new}} = C_{layer\,pair} + (C_{resistor\,material})(N_{up_{new}})\sum_{i=1}^{N_{R'}} Area_{R_i} + N_{R'} C_{trim} N_{up_{new}} + C_{print} \quad (13)$$

where the sum in (13) is taken over all embedded resistors in the particular layer pair of interest ($N_{R'}$), and

$C_{resistor\,material}$ = cost per unit area of the resistive material printed on the wiring layers to create embedded resistors

C_{trim} = the average cost of trimming one printed resistor

C_{print} = the average cost of printing or plating all embedded resistors onto one layer pair.

The board price is combined with component-specific assembly, test, and rework costs to determine the system cost. The average effective cost associated with a single instance of a discrete passive is computed as follows:

$$\begin{aligned} C_{discrete} = {} & P_{discrete} + C_{handling} + C_{assembly} + C_{AOI} \\ & + (1 - Y_{assembly})(C_{assbly\,rework} + P_{discrete} + C_{handling}) \\ & + (1 - Y_{functional})(C_{func\,rework} + P_{discrete} + C_{handling}) \end{aligned} \quad (14)$$

where

$P_{discrete}$ = purchase price of a discrete passive component

$C_{handling}$ = storage and handling costs associated with a discrete passive component

$C_{assembly}$ = the cost of assembly of a discrete passive component (per site)

C_{AOI} = cost of inspecting a discrete passive component (per site)

$Y_{assembly}$ = assembly yield for discrete passive components

$Y_{functional}$ = functional yield of discrete passive components

$C_{assbly\,rework}$ = cost of reworking an assembly fault (per site)

$C_{func\,rework}$ = cost of diagnosing and reworking a functional fault.

The $(1\text{-}Y_{assembly})$ term in (14) represents the fraction of discrete passives requiring rework (replacement) due to assembly faults. The $(1\text{-}Y_{functional})$ term in (14) represents the fraction of discrete passives requiring rework (replacement) due to functional faults.

Equation (14) assumes that all assembly and functional faults associated with discrete passives are diagnosable and reworkable.

The total system cost (for relative comparison purposes only) is given by,

$$C_{system} = \sum_{i=1}^{N_{discrete}} C_{discrete\,i} + P_{board} \tag{15}$$

where

$C_{discrete_i}$ = the cost associated with the ith discrete passive component from (14)
P_{board} = the board price from (11) or (12)
$N_{discrete}$ = number of discrete passive components assembled on the board.

Note, the following costs are not included in the formulation because they are assumed to be the same whether or not the system contains embedded passives: all functional testing costs are ignored, all costs associated with other non-embeddable system components are ignored.

13.3.3 Throughput

A fundamental issue that has to be addressed for embedded passives is the throughput of the process that is used to manufacture the boards. Throughput is a measure of the number of products that can be produced in a given period of time, and is the inverse of the inter-departure time (the time elapsed between completed products). Throughput is key to understanding the profit margin that will be required to justify manufacturing embedded passive boards. The objective of this portion of the analysis is the computation of application-specific relative profit margin values for conventional and embedded passive versions of a board.

The situation faced by the board manufacturer may be the following: assume that there are two types of boards that could be fabricated on a process line, one is a conventional board with a known profit margin and the other is an embedded passive board. To simplify the problem, assume that the number of boards to be manufactured will be the same for both types of board. The manufacturing cost of the embedded passive board will be larger. Assuming the inter-departure time of the embedded passive process will be longer than that for conventional boards, the manufacturer must decide what profit margin to use for the embedded passive board so that the total profit per unit time made by selling embedded passive boards equals or exceeds what can be made by selling the conventional boards. This is necessary to justify the use of a line to fabricate embedded passive boards when it would otherwise be producing conventional boards.

To explore throughput effects and determine the relative profit margins of the printed circuit boards, a model has been developed that is similar to cost of ownership models for capital equipment (e.g., [13]). The model captures the costs due to maintenance

(scheduled and unscheduled), yield loss, inter-departure time variations, and change overs.

The labor costs associated with scheduled and unscheduled maintenance, and change overs are given by (16),

Scheduled Maintenance: $$L_{sm} = N_{sm} T_{sm} R_L \quad (16a)$$

Unscheduled Maintenance: $$L_{usm} = \frac{MTTR}{MTBF}(T_{total}) R_L \quad (16b)$$

Change Overs: $$L_{co} = N_{co} T_{co} R_L \quad (16c)$$

where

N_{sm} = number of scheduled maintenance activities in a given period of time
T_{sm} = average labor time (touch time) associated with a scheduled maintenance activity
N_{co} = number of change overs in a given period of time
T_{co} = average labor time (touch time) associated with a change over
R_L = labor rate
MTTR = Mean (labor) Time To Repair for an unscheduled maintenance event
MTBF = Mean Time Between Failures (unscheduled maintenance)
T_{total} = total time in the period of interest.

We must now evaluate the throughput impacts of various critical manufacturing events. Computed throughput loss is basically determining lost opportunity costs, i.e., how much good product does not get manufactured because the process has been slowed or stopped, or because defective product is produced instead. We assume that scheduled maintenance does not affect the throughput, i.e., it is performed during periods when the process would not be operational, therefore, only the cost of performing the scheduled maintenance is important for our tradeoff, also we assume that the scheduled maintenance periods for lines producing conventional and embedded passive boards are of the same length and occur at the same frequency. Note, if there is no effective off-shift (i.e., no time when maintenance can be performed that does not effect the throughput), then N_{sm} is set to zero and all maintenance is treated as unscheduled maintenance.

The throughput impact of process yield can be computed from the number of multilayer panels lost in a fixed time period due to process yield losses,

$$Lost_{yield} = (1 - Y_{ilp}) \frac{N_{inner\ layers}}{N_{inner\ layers\ per\ board}} \quad (17)$$

where

Y_{ilp} = yield of the panel inner layer process

$N_{inner\ layers}$ = number of panel inner layers produced in a fixed time period
$N_{inner\ layers\ per\ board}$ = number of inner layer pairs in a single board.

Unscheduled maintenance, assuming it is performed during time when the process line would otherwise be producing good product contributes the following lost time,

$$\mathrm{Lost}_{usm} = \left(\mathrm{MTTR} + 2\mathrm{T}_{c/s}\right)\frac{\mathrm{T}_{total}}{\mathrm{MTBF}} \tag{18}$$

where $T_{c/s}$ is the cool down/startup time associated with the line being stopped for the unscheduled maintenance activity. Similarly, the change overs result in lost opportunity to produce products,

$$\mathrm{Lost}_{co} = \mathrm{N}_{co}\left(\mathrm{T}_{co} + 2\mathrm{T}_{c/s}\right) \tag{19}$$

Knowing the inter-departure time, the average number of multilayer boards that can be obtained from the process line during the time period defined by T_{total} is given by,

$$\mathrm{N}_{boards} = \left[\frac{\mathrm{T}_{total}}{\mathrm{T}_{inter}\mathrm{N}_{inner\ layers\ per\ board}}\left(1 - \frac{\mathrm{Lost}_{usm} + \mathrm{Lost}_{co}}{\mathrm{T}_{total}}\right) - \mathrm{Lost}_{yield}\right]\mathrm{N}_{boards\ per\ panel} \tag{20}$$

where
T_{inter} = inter-departure time of the inner layer process (time/inner layer pair)
$N_{boards\ per\ panel}$ = number up, i.e., the number of boards that can be fabricated on a panel.

The parameter that needs to be evaluated for comparison purposes is the total profit in a fixed period of time from fabricating a specific board type. Note, the profit per board is not a good comparison metric because it does not account for the number of boards that are produced. The average profit in the time period associated with the constituent variables is computed from,

$$\mathrm{Average\,Profit} = \mathrm{N}_{boards}\mathrm{V} - \left(\mathrm{L}_{sm} + \mathrm{L}_{usm} + \mathrm{L}_{co}\right) \tag{21}$$

where the value of a board (V) is given by,

$$\mathrm{V} = \left(1 + \mathrm{M}\right)\mathrm{C}_{board} \tag{22}$$

where
M = profit margin
C_{board} = manufacturing cost per board.

The example results shown in Figure 2 were generated using the model described by (16)-(22). If inter-departure times of inner layer production for conventional and

embedded passive layers, and the average profit margin for conventional boards are known, then the minimum required profit margin for embedded passive board fabrication can be determined. Note, this cost model must be repeated for each board manufacturing scenario since the number of layers in the multilayer board and the dimensions of the individual board are application-specific.

The example shown in Figure 2 indicates that if, conventional boards have a 15.7% profit margin and 15 second inter-departure time (per layer pair), then 30 second per layer pair embedded passive board production is only feasible for profit margins of 26% or more. The most important property obtained from this analysis is the difference between the profit margins, the tradeoff analysis results are much less dependent on the absolute values of the profit margins. We consistently observe profit margin differences of ~10%. The analyses presented in Section 13.4 assume profit margins that make the average profit per hour of each type of board fabrication equal.

Additional throughput and manufacturing modeling impacts such as manufacturing cycle time and capacity analysis for embedded passive board manufacturing appears in [14].

13.3.4 Trimming Embedded Resistors

Laser trimming of film resistors has been performed for many years. For many applications (depending on design tolerances) embedded resistors will need to be trimmed. Resistors are trimmed by machining a trough in the resistive element, the

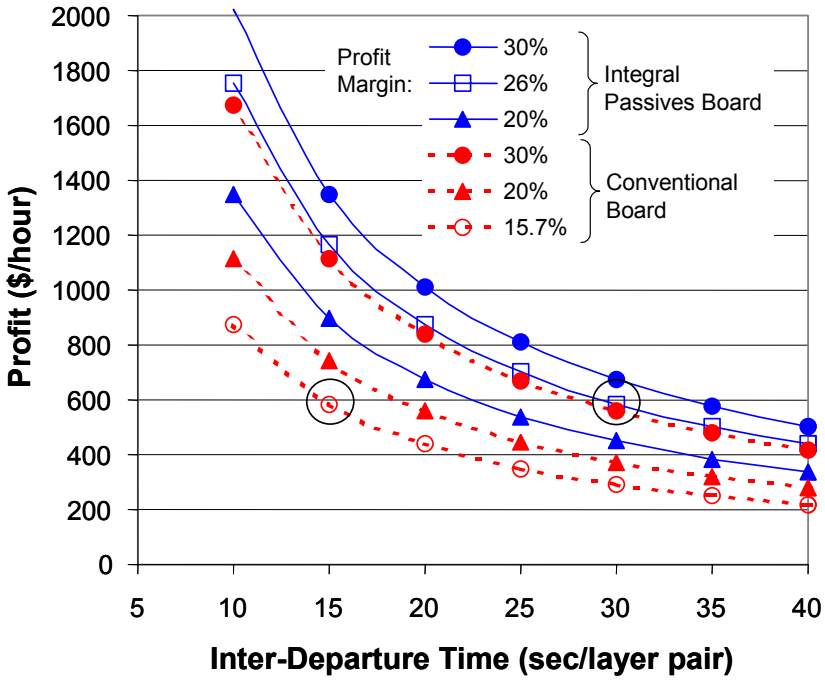

Figure 2 - The relationship between profit margin and production inter-departure time for conventional and embedded passive board fabrication.

length and path-shape of which determine the resistance change obtained (Chapter 2).

It is also possible to consider reworking embedded resistors prior to completion of the board fabrication process (Chapter 3). Resistors may be reworked because their initial value is too large due to either trimming errors or original fabrication (trimming can only increase the resistance of a resistor). One method of reworking embedded resistors is to print conductive ink on the surface of an embedded resistor thus adding a lower value parallel resistor that effectively "trims down" the resistor value, [15].

A cost of ownership model for a laser trimming process has been developed by ESI, [16]. The ESI model allows the amount of time to trim a layer pair to be computed as a function of the number of resistors to be trimmed per layer pair and the size of the panel (laser trimming throughput). A version of the ESI model is used in the analysis process shown in Figure 1 (Step 6).

Unfortunately, trimming and rework equipment is expensive and both processes potentially represent bottlenecks in the board fabrication process. Therefore, the question that naturally arises is, under what conditions (application properties and resistor fabrication process) is it economically feasible to perform trimming and possibly rework versus disposal of layer pairs or boards that do not meet design specifications?

When resistors are fabricated the resulting values form a distribution, Figure 3. If the resistors are to be trimmed, the fabrication target resistance (peak of the distribution) is below the application target resistance so that the greatest number of fabricated resistors can be trimmed to values in the specified range. The High Specification Limit (HSL) and the Low Specification Limit (LSL) are determined from the design tolerance associated with the resistor. The area under the curve between the HSL and the LSL

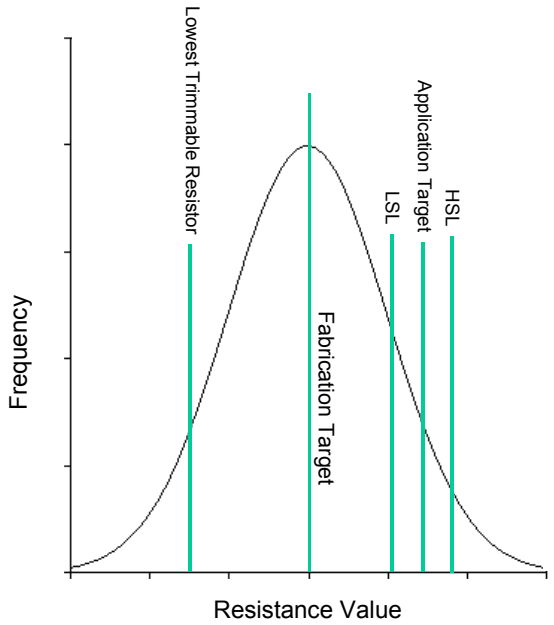

Figure 3 – Distribution of fabricated resistor values.

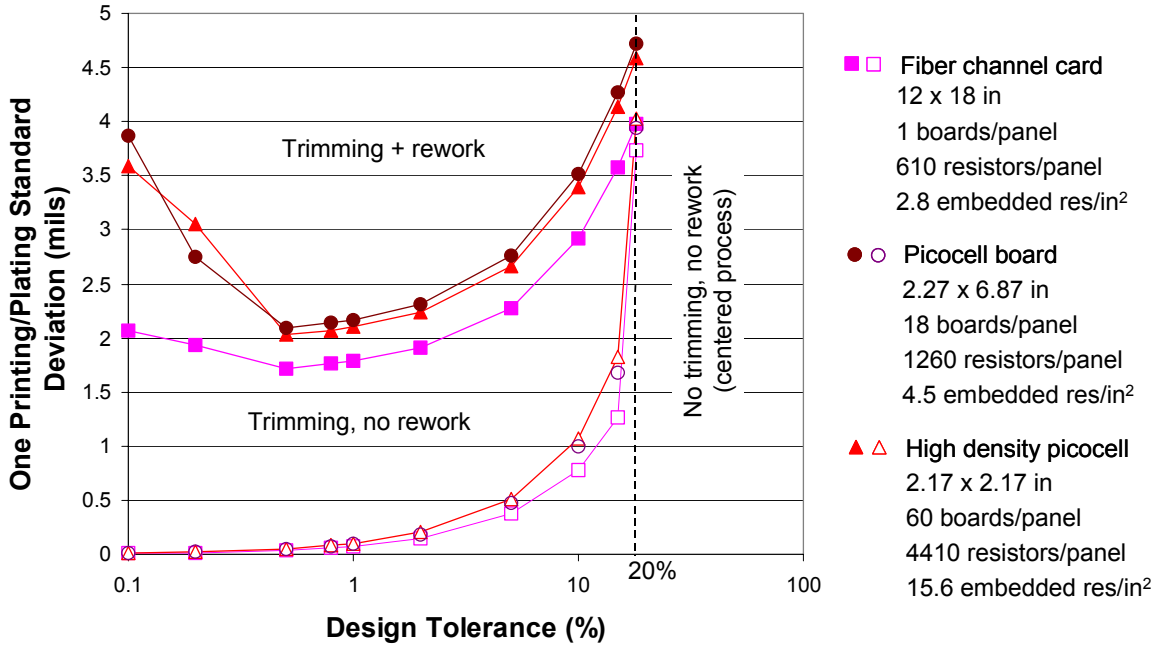

Figure 4 – Application-specific economical regions of trimming and reworking embedded resistors. This example result assumes no resistor thickness variation, see [17] for additional assumptions and modeling parameters associated with this result.

represents the yield of the untrimmed resistor. There is a lower limit to the ability to successfully trim a resistor that is approximately 55% of the application target. The area between the lower trimming limit and HSL represents the yield of trimmed resistors (assuming no trimming defects). Resistors in the distribution that have values below the lower trimming limit or above HSL would generally be considered yield loss (unusable and untrimmable). Rework allows resistors above HSL to be recovered and used. In cases where no trimming is planned, the process would be centered so that the fabrication target and the application target are the same.

Figure 4 shows the result using the model developed in [17] for three different applications. The three regions identified in Figure 4 provide the conditions under which it is most economical to trim, trim and rework, and simply scrap non-conforming inner layer pairs.

13.3.5 Yield and Test

The discussion in Section 13.2 rolls in the assembly and functional yield of discrete passives, e.g., (14). The critical yield parameter not explicitly considered is the board yield (see Chapter 8). The foregoing discussion effectively assumes that the layer pair cost with embedded passives, $C_{\text{layer pair}_{\text{new}}}$, computed in (13) is a yielded cost, i.e., the cost per good (non-defective) layer pair, [18]. This quantity can be interpreted as yield

cost (manufacturing cost/yield) only if we assume that all the defective embedded passive layer pairs can be identified and removed from the production process before they are incorporated into multilayer boards.

If the yield of the embedded passive layer pairs going into board layup and lamination is not 100%, then we assume that some fraction of the defects will be detected at some later point during the board fabrication, system assembly, or final test. Obviously the cost impact of undetected defective embedded passive layer pairs is greater, the later in the process they are discovered. The following simple exercise demonstrates this, consider the outgoing cost per assembled board from the final in-circuit test step that discovers a defect caused by an embedded passive layer pair,

$$C_{out} = \frac{C_{in} + C_{test}}{Y_{in}^{f_c}}, \tag{23}$$

where C_{in} is the total investment in the board and assembly prior to the test, C_{test} is the cost of performing the in-circuit test, Y_{in} is the yield of the board coming into the test, and f_c is the fault coverage of the test. As an extreme case, assume that $C_{in} = C_{board} + C_{assmbly\ \&\ components}$ = \$100 + \$50 = \$150 has been invested in a board and assembly, the test costs C_{test} = \$7.50 to perform per assembly, the yield of the assemblies is Y_{in} = 0.8 or 20 out of every 100 assemblies are defective (assume all the defects are the result of defective embedded passive layer pair and assume further, for simplicity, that we are fabricating only one board per panel), and f_c = 0.9 (90% of the defects are successfully detected by the in-circuit test). Then the outgoing cost per good board is effectively C_{out} = \$192.53. This result assumes that all the defective assemblies are scrapped (disposed of) and none can be reworked. Note, the yield of assemblies that pass the test is given by,

$$Y_{out} = Y_{in}^{1-f_c}, \tag{24}$$

so for our example case, the yield out of the test activity is Y_{out} = 97.79% (2.21% test escapes). The final yielded cost of the assemblies is C_{out}/Y_{out} = \$196.88. If, on the other hand, the defective embedded passive layer pair had been detected prior to its lamination into the multilayer board, applying (23) during the board fabrication assuming that \$20 was spent on the embedded passive layer pairs that are 80% yield and we have a 90% fault coverage test (assume the test costs \$2/layer pair), the effective embedded layer pair cost would be \$26.89 (the total board cost would now increase to \$106.89, but the yield also increases to 97.79%). Now applying (23) and (24) with an incoming yield of 97.79% instead of 80% at assembly gives us, C_{out} = \$160.08, Y_{out} = 99.78%, and C_{out}/Y_{out} = \$160.43 (much less than the original case that did not detect the defective board until assembly began). While this is obviously a very oversimplified case, the point is that layer pair yield will have a different effect on the system manufacturing cost depending on where in the process you are able to detect the problem.

In general, embedded passives represent increased complexity (possibly increased layer count) in the board, which translates into a greater probability of test escapes at the bare board level leading to more scrapping at the assembly level. To summarize, the economic viability of using embedded passives in some applications may lie in how accurately defects can be detected at the layer pair level prior to completion of the board and assembly.

13.3.6 Life Cycle Costs

Thus far we have only considered system manufacturing and size issues. This only represents a portion of the economic impacts of converting discrete to embedded passives. Life cycle effects, which for many applications will dominate manufacturing costs, include all other activities associated with the product. Generally speaking, life cycle effects are more difficult to quantify into costs than manufacturing activities. Life cycle activities include:

Design Costs – Costs of engineering and other technical personnel to design boards that include embedded passives. If designers require specialized training, or new CAD and/or other specialized design tools to successfully perform embedded passive board design, then the costs of these activities must be considered. A summary of the design tool requirements for embedded passives is included in the NEMI 2002 Industry Roadmap, [19]. One must also consider costs associated with effort and tools for design verification and functional test development. Extra design costs may also include libraries of models for embedded passives ranging from symbol libraries to high-performance RF models for use in electrical simulation. The inclusion of embedded passives may also affect the degree to which a design can be reused and upgraded (re-design costs). Also included in the design costs are prototyping costs. Are embedded passive applications going to require additional prototype boards?

Non-Recurring Costs – To what extent will embedded passives require board fabricators to invest in new equipment (see [7] for an equipment analysis)? Equipment is not the only non-recurring cost that may be associated with embedded passives. There will be additional tooling (artwork) for layer pair production, potentially additional chemistry to be managed in the board fabrication process, and finally licensing fees and royalties may have to be paid for the use of technology, material, and/or processes.

Time-to-Market – Does the design, verification, and prototyping of embedded passive boards require more calendar time than that for conventional systems? Delays in time-to-market for a new product of weeks or months can cost substantial money and in some cases mean missing the market for the product completely. See [20] for a typical time-to-market cost model that forecasts revenue as a function of delays in time to market and the length of the market window.

Performance Value – Embedded passives may result in size or performance improvements in a systems that enable increases in market share for the manufacturer.

It may be the case that for some quantifiable increase in system cost, a manufacturer can differentiate itself from its competition by providing a product that is lighter, smaller, faster, more reliable, or with greater functionality than its competition, and the customer is willing to pay extra for one or more of these improvements. This type of value increase can be mapped to a life cycle cost, however, it requires a business oriented financial modeling capability.

Qualification and Certification – The introduction of new materials and processes into board fabrication requires material providers and board fabricators to assess and possibly update safety certifications, e.g., UL Certification. While the cost of this type of certification is not directly borne by the users of embedded passives, it will be reflected in the board costs. On the other hand, there will be a reduction in the costs associated with qualifying discrete component manufactures.

Liability – Embedded passives, or any new technology, material, or process may carry with it unforeseen financial liabilities. The liabilities may be in the form of causing injury to customers, employees of the manufacturer, or the environment. Long-term studies of the effects of the materials and the processes used to incorporate them into boards may be necessary to prove or disprove liability claims.

Sustainment – Sustainment is a collection of many activities all of which have an economic impact. In general, sustainment is all the activities necessary to:

- keep an existing system operational (able to successfully complete the purpose it is intended for);
- continue to manufacture and field versions of the system that satisfy the original requirements;
- manufacture and field new versions of the system that satisfy evolving requirements.

The foremost concern with embedded passives is reliability. Conventional wisdom is that system reliability will improve because of the reduction in the number of solder joints, however, this will only be realized if the reliability does not commensurately decrease due to other embedded passive specific effects. Reliability questions arise from two origins: first are the specific embedded structures as reliable or more reliable than the rest of the components and packaging? Secondly, are there embedded passive specific processing conditions (during board fabrication) that remove life from other conventional board structures? Changes in system reliability appear either as warranty costs (replacement) or as maintenance costs (repair). General warranty cost models appear in [21].

For systems that are subject to repair, embedded passives may change the ease with which problems in the system can be diagnosed, physically repaired and retested. In turn, if the faulty board is to simply be replaced, its reliability impacts the number of “spare” boards that must be manufactured to fulfill expected replacement commitments.

Sustainment, however, goes further than reliability driven replacement and repair. Sustainment also means that the system should remain manufacturable through the end of its support life (to fulfill additional requirements for new product and spare replenishment). This is not generally difficult for manufacturers of laptop computers and other short-life consumer products, but is a huge concern (and cost issue) for long-life products such as avionics for aircraft. The biggest component related problem that long field life systems see is obsolescence (particularly electronic part obsolescence), [22]. Most electronic parts have short lifetimes (from an availability perspective) relative to even the design cycle of an aircraft, let alone an aircraft's support life. For systems like aircraft, qualification and certification requirements may make simple substitution for obsolete parts with newer parts prohibitively expensive. Embedded passives will mitigate some obsolescence problems by replacing discrete parts that would become obsolete. On the other hand, if the materials used to manufacture the embedded passives within the board become obsolete, i.e., replaced by newer materials, the overall obsolescence problem may well become much worse. Models for the application-specific economic impact of part obsolescence appear in [23].

Environmental and End of Life – The fabrication of passives within boards obviously increases the volume of waste produced during the board fabrication process. Disposition of board fabrication waste is a significant contributor to the price of boards. If any of the embedded passive specific contributions to the waste steam are considered hazardous then the waste disposition costs could increase significantly. Waste disposition is also a factor at the other end of the life cycle, i.e., at end-of-life. Depending on the type of product that the embedded passive board is being used within and the location in the world where the product is being sold, the manufacturer may bare some or all of the cost of disposing of the product when the consumer has finished with it, e.g., television sets in Germany.

Financial – Several costs associated with creating and holding inventory (handling, storage, procurement) associated discrete passives are potentially avoided, this includes the cost of money that is invested in stored passives as opposed to invested elsewhere.

13.4 Example Case Studies

In this section we present the results of size/cost tradeoff analyses performed on several different single board applications, including a picocell board, the NEMI hand-held emulator and a fiber channel card. It is not the intent of these analyses to prove that embedded passives lead to less expensive systems, rather we wish to understand the economic realities should we decide to use embedded passives. The following case studies only include manufacturing costs (no life cycle effects are included).

The relevant characteristics of the applications are given in Table 1. The common data assumptions for both applications are shown in Table 2.

TABLE 1. PICOCELL BOARD, HAND-HELD EMULATOR AND FIBER CHANNEL CARD APPLICATION CHARACTERISTICS

	Picocell Board	**Hand-Held [19]**	**Fiber Channel Card**
Number of Embeddable Discrete Resistors	27 (< 100 Ω) 19 (100-1000 Ω) 22 (1 – 10 kΩ) 1 (10 – 100 kΩ) 1 (>100 kΩ)	40 (<100 Ω) 134 (0.1 – 1 kΩ)	210 (< 100 Ω) 181 (100-1000 Ω) 150 (1 – 10 kΩ) 63 (10 – 100 kΩ) 6 (>100 kΩ)
Size of Embeddable Discrete Resistors	69 0805 (80x50 mils) 1 1201 (120x100 mils)	0402 (40 x 20 mils)	561 0603 (60x30 mils) 10 0805 (80x50 mils) 31 120x60 mils 8 250x120 mils
Number of Embeddable Discrete Capacitors	1 (< 100 pF) 29 (100 – 1000 pF) 13 (1 – 10 nF)	69 (<100 pF) 40 (100 - 1000 pF)	88 (0.001μF) 38 (0.01μF) 116 (0.1μF)
Size of Embeddable Discrete Capacitors	0805 (80x50 mils)	0402 (40 x 20 mils)	159 0603 (60x30 mils) 82 0805 (80x50 mils)
Discrete Passive Cost	$0.0045 per part	$0.0045 per part	$0.0045 per part
Conversion Cost (excluding assembly)	$0.015 per part	$0.015 per part	$0.015 per part
Board Size	2.27 x 6.87 inches	30 cm^2 (square board assumed)	12 x 18 inches
Number of Board Layers	10	6	12

TABLE 2. DATA ASSUMPTIONS USED IN THE MODELING

Panel Fabrication	**Throughput Analysis**	**Embedded Passives**
Panel size = 18 x 24 inches (except where otherwise noted)	Change overs = 4/week	Capacitance layer: 10 nF/cm^2
Edge scrap = 0.75 inches	Change over time = 15 minutes	Resistive material: 200 ohms/square
Min. spacing between boards = 0.15 inches	Cool down and start up = 30 minutes	Minimum feature size for embedded components = 15 mils
Cost per layer pair = $\$12.50/ft^2$	MTBF = 200 hours (conventional) MTBF = 150 hours (embedded passive)	$C_{resistor\ material}$ = $\$0.08/in^2$
	MTTR = 1 hour	C_{trim} = $0.002/embedded resistor
Assembly	Labor rate (repair) = $25/hour	C_{print} = $7.43/layer pair
Min. Assembly Spacing = 20 mils	Production hours = 5000/year	Cost of capacitor layer material = $\$14.40/ft^2$ (>10 nF/in^2)
Yield = 0.992/discrete passive [6]		Spacing between non-bypass embedded capacitors (S_c) = 50 mils
Cost = $0.0045/discrete passive	**Routing Analysis**	
AOI = $0.0001/discrete passive	Average fanout = 2.1	
Assembly Rework = $4/site [6]		
Functional Rework = $4/site [6]		

13.4.1 Picocell Board Application

Figure 5 shows analysis results for the picocell board as discrete resistors are replaced by embedded resistors (capacitors are not integrated in Figure 5). Relative system cost is plotted in Figure 5 and throughout this section indicating the system cost less the cost of all non-embeddable components and functional testing. The specific solution (data points) in Figure 5 indicate that the embedded passive board becomes economical

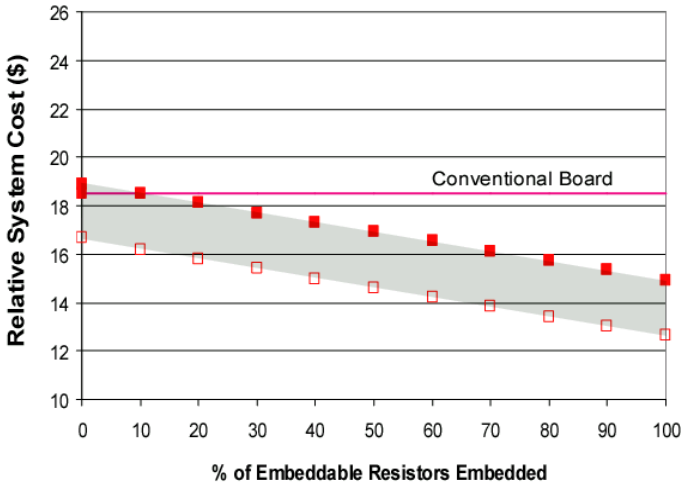

Figure 5 - The economics of embedded resistors for the picocell board application. Each data point represents the embedded passive solution for a specific routing resource assumption (assumption of the ratio of resources actually used to route the conventional implementation of the board and the theoretical maximum amount of resources that could be used), the band represents all possible embedded passive solutions for this application; the solid horizontal line is the system cost of conventional implementations. Only resistors ≤ 10 Kohms were considered embeddable.

when approximately 10% of the embeddable discrete resistors are embedded[3]. The data point at $18.30 when no resistors are embedded represents the board price increase due only to the need for a higher profit margin to justify embedded passive board fabrication (see Section 13.3.3). The next point on the vertical axis (~$19.00) is the relative cost of the system when the first resistor is embedded.

The resistor results appear as a "band" in Figure 5 due to the range of values that U_{conv}/U_{limit} can take on in (5). The upper edge of the band (the closed data points in Figure 5), represents the assumption that the conventional board used all available routing resources efficiently, i.e., U_{conv}/U_{limit} is close to 1.0. The lower edge of the band (the open data points in Figure 5), represents the assumption that the conventional board made poor use of the available routing resources, i.e., U_{conv}/U_{limit} is smaller.[4] Practically speaking, all solutions start at the top edge of the band (10 layers for the picocell board) and may step down to the lower edge of the band (8 layers for the picocell board) at some point depending on the actual value of U_{conv}/U_{limit} for the application. Another type of step discontinuity can also appear in the results if the board shrinks in size enough so that more boards can be fabricated on a panel. In the picocell

[3] The embedded resistors considered in this study are considerably more economical than embedded resistors in previous studies due to the assumption of fabrication of the embedded resistors directly on wiring layers as opposed to dedicated embedded resistor layer.

[4] The minimum value is determined by finding the smallest value of U_{conv}/U_{limit} that predicts the correct number of layers in the conventional solution.

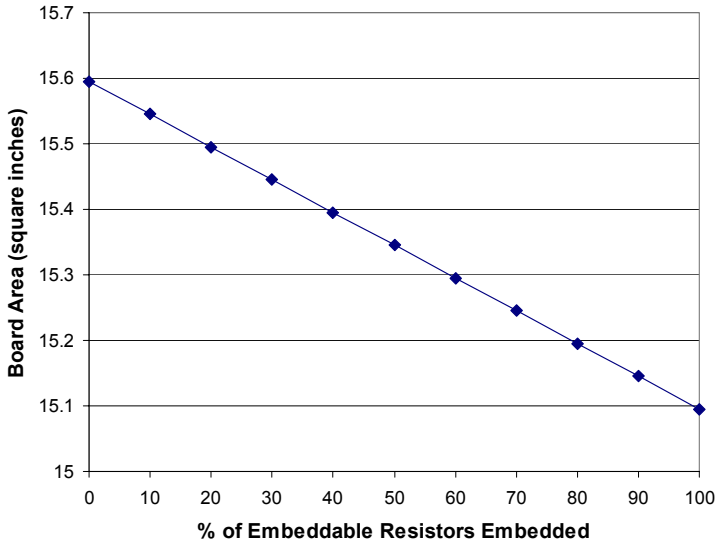

Figure 6 - Board size decrease with resistor embedding for the picocell board application.

board case, the board size never decreases sufficiently to allow more boards to be fabricated on an 18 x 24 inch panel, however, potential board size decreases are still important to the customer of this board and Figure 6 shows the board area change as fraction of embedded resistors is varied.

Next consider the integration of capacitors. Figure 7 shows the relative system costs as the embeddable capacitors are integrated (none of the embeddable discrete resistors are embedded in Figure 7). Since embedding of bypass capacitors requires material replacement and non-bypass capacitors requires the addition of an extra layer pair (for the technologies we assumed), the very first bypass capacitor embedded increases the cost of the board dramatically, but as more capacitors are embedded, the added cost of the replacement material layer is gradually offset by the avoidance of discrete capacitor part and assembly costs. The driver that determines whether capacitor embedding is economical or not, is the density of embeddable discrete capacitors on the board. Figure 8 shows that if additional embeddable capacitors were added to the picocell board application (thus increasing the capacitor density), bypass embedded capacitors would become economically viable at approximately 6.9 capacitors/square inch, whereas the actual picocell board application has only 2.76 capacitors/square inch.

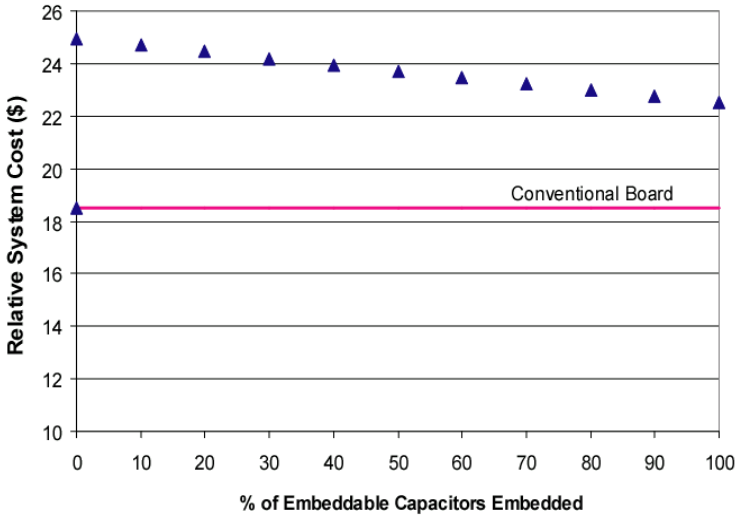

Figure 7 - Capacitor embedding for the picocell board application. Only capacitors ≤ 100 nF were considered embeddable.

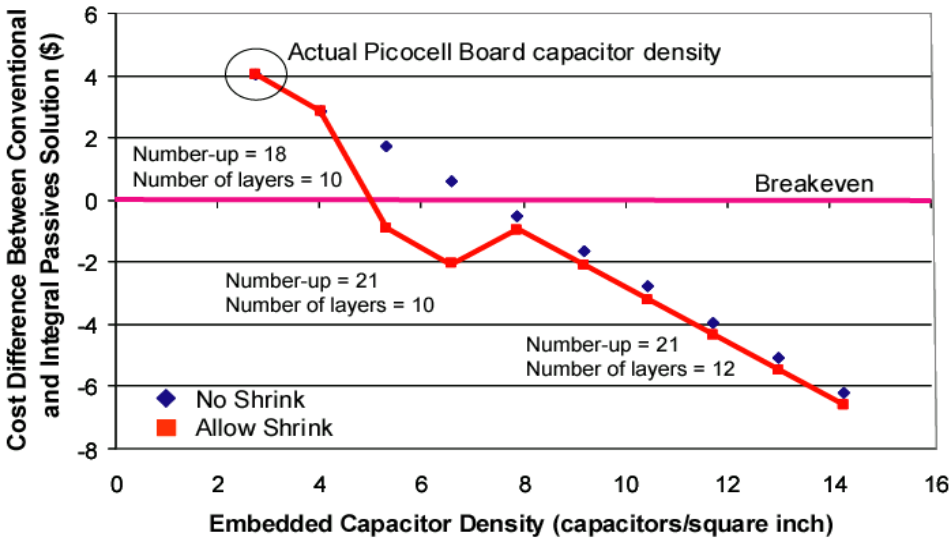

Figure 8 - The impact of embeddable capacitor density on system cost for the picocell board application. When the density of embeddable bypass capacitors is increased, the number-up first decreases due to the decreased board size (if the size is allowed to change), and later (as density increases) a layer pair addition is required to support routing requirements of the application with the smaller board size.

13.4.2 NEMI Hand-Held Product Sector Emulator

Analyses similar to those performed for the picocell board have been applied to the NEMI hand-held emulator described in Table I. Figure 9 indicates that the embedded

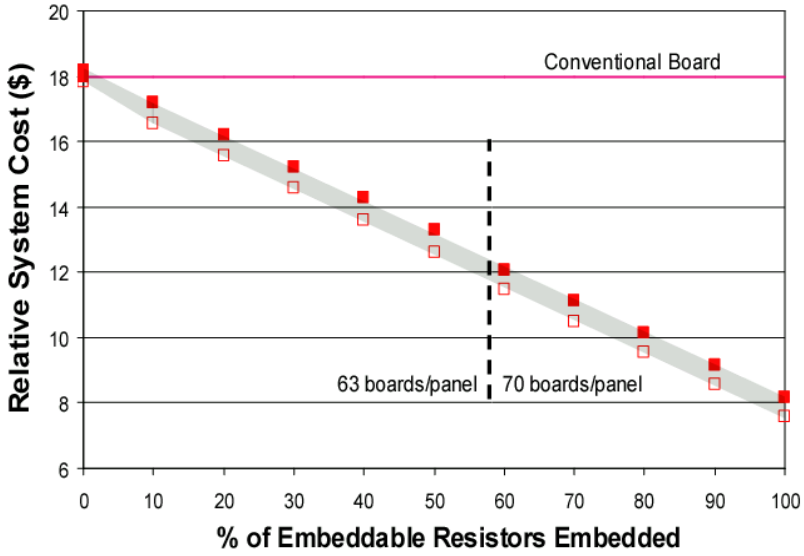

Figure 9 - The economics of embedded resistors for the NEMI hand-held product sector emulator (5.5 x 5.5 cm board fabricated on an 18 x 24 inch panel). The data points represent specific embedded passive solutions; the solid horizontal line is the relative system cost of the conventional implementation.

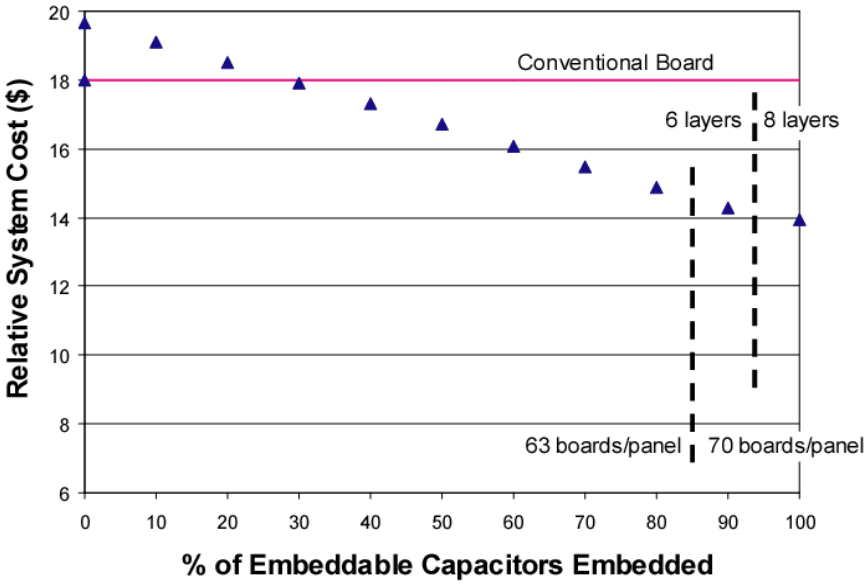

Figure 10 - Capacitor embedding for the 5.5 x 5.5 cm NEMI hand-held product sector emulator. No embedded resistors are fabricated in this example. The baseline for this plot (the horizontal line) is the board with none of the embeddable capacitors embedded.

passive board becomes economical when approximately 3% of the embeddable discrete resistors are embedded. A discontinuity in the embedded passive board data is labeled on the plot. The discontinuity appears when enough resistors have been

embedded to sufficiently reduce the board size so that additional boards can be manufactured on the panel (number-up increases). In the hand-held emulator case, the boards are small (i.e., the number-up on the panel is large) and the overall price of the boards is low (under $2/board), therefore the effect of increasing the number-up has a minimal effect on the system cost.

Figure 10 shows the relative system costs as the embeddable capacitors are integrated (none of the embeddable discrete resistors are embedded in Figure 10). When bypass capacitors are embedded, the cost initially increased by the material replacement cost. We have assumed that when a bypass capacitance layer pair is added, less total bypass capacitance will be necessary, Chapter 12. Note, a much better economic case can be made for embedded bypass capacitors in the hand-held emulator than for the picocell board due to the larger embeddable bypass capacitor density (23.44 capacitors/square inch). Similar to the embedded resistor characteristics, eventually enough bypass capacitors are embedded to reduce the size sufficiently to allow a number-up increase (note, there are fewer embeddable capacitors than resistors, so the this discontinuity occurs later in the embedding process than for resistors). Also note that a second discontinuity appears in Figure 10 – a layer change. As board area decreased, so did the available wiring resources, eventually an additional layer pair had to be added to interconnect the system components.

13.4.3 Fiber Channel Card

Figures 11 and 12 show the results of embedding resistors and bypass capacitors into the fiber channel card described in Table I. In this case the board is large and only one can be fabricated per panel (results for two different panel sizes are considered in Figures 11 and 12). Because all the cost associated with fabricating embedded resistors on a panel has to be born by a single board, 25-35% of the 610 embeddable resistors need to be embedded to realize a cost savings. Figure 11 also shows that when there is less panel waste (i.e., when the board is fabricated on a smaller panel), embedded resistors become economical more quickly.

Figure 12 shows the effect of integrating bypass capacitors for the fiber channel card. For this example there are only 242 embeddable capacitors on a 12 x 18 inch board (1.12 embeddable capacitors per square inch). As indicated in the hand-held and picocell examples, with such a low embeddable capacitor density it is not likely to be economical to embed the capacitors.

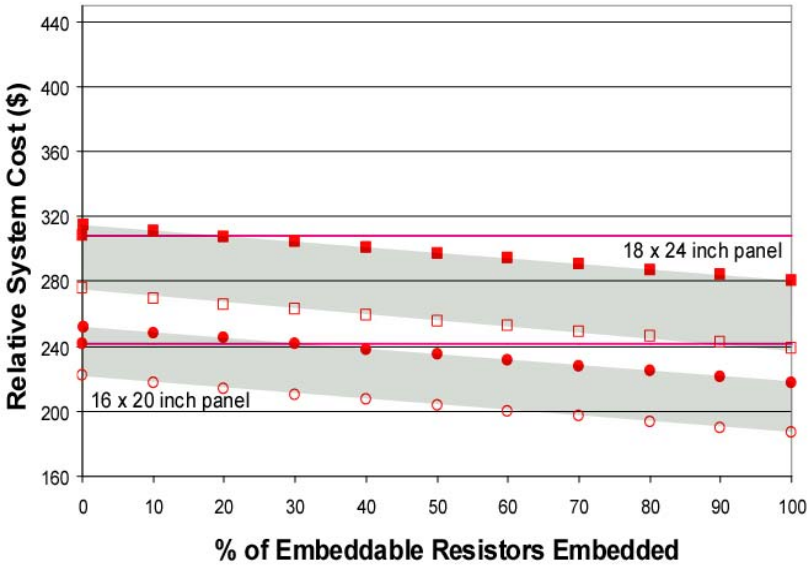

Figure 11 - The economics of embedded resistors for the fiber channel card. The data points represent embedded passive solutions; the solid horizontal lines are relative system costs of conventional implementations.

The economics of embedded bypass capacitors can be generalized by observing the application-specific embeddable capacitor density necessary to breakeven on costs, i.e., by plotting the embeddable capacitor densities where the cost difference between the conventional and embedded passive implementations is zero (for the picocell board application this point is 6.9 embeddable bypass capacitors per square inch from Figure 8). Figure 13 shows the general result for the three applications considered in this chapter. The critical assumptions for this plot are: the board size and the number of layers required for routing is not allowed to change. The primary differentiator between the applications as far as this plot is concerned is the panelization efficiency (the total board area on the panel divided by the panel area). The dielectrics used to produce embedded capacitor layers are relatively expensive and would be purchased and used at the panel size, therefore, a low panelization efficiency indicates that the application is wasting a lot of the expensive material, versus a larger panelization efficiency indicates less waste and therefore lower breakeven capacitor densities are possible.

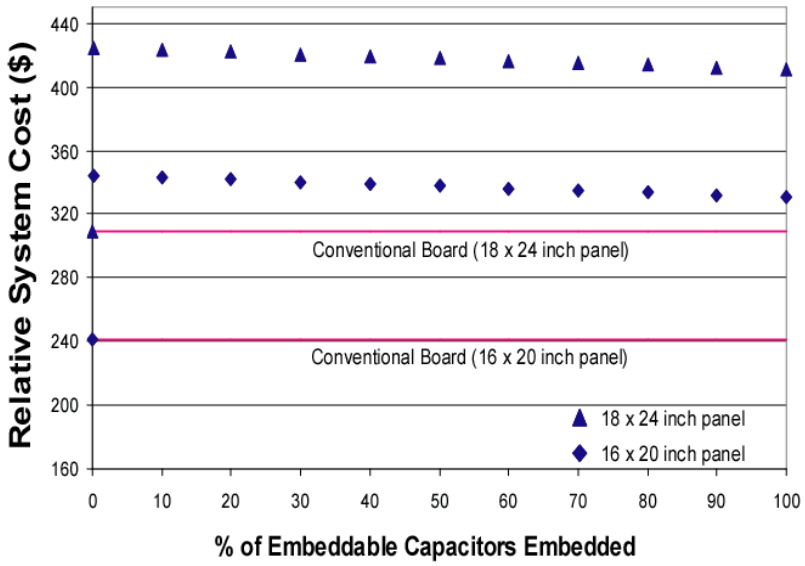

Figure 12 - Capacitor embedding for the fiber channel card. Note, in this case there are no embeddable discrete non-bypass capacitors.

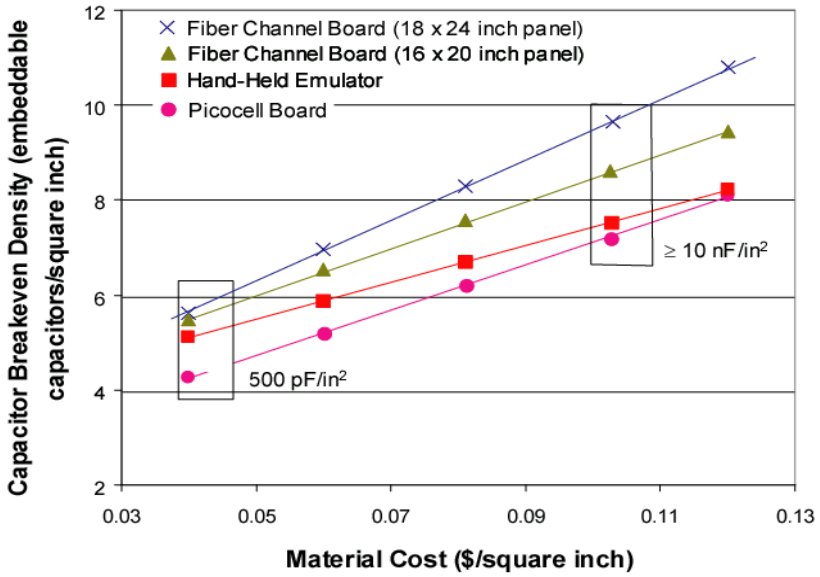

Figure 13 - Bypass capacitor breakeven densities as a function of dielectric material replacement costs. Only single layer substitution is considered in this plot. The actual capacitor densities: Fiber Channel Board – 1.12 caps/in^2, Picocell Board – 2.76 caps/in^2, NEMI Hand Held Emulator – 23.44 caps/in^2.

13.5 Summary

In this chapter we have presented the results of an application-specific economic analysis of the conversion of discrete passive components (resistors and capacitors) to embedded passives that are embedded within a printed circuit board. The model has

been demonstrated on a picocell board, the NEMI hand-held emulator, and a fiber channel board. In these cases, we found embedded resistors to be generally cost effective with the most significant economic impact resulting from either number-up increases due to board size reductions, or layer count decreases due to reductions in routing requirements. Because we considered embedded resistors fabricated directly on wiring layers (as opposed to dedicated embedded resistor layers assumed in previous studies [6] and [7]), we can not generalize to components per unit area because the results are driven by the board fabrication profit margin (profit margin is a fractional increase in board cost and thus much smaller in absolute terms for high number-up), whereas cost reduction is through omission of discrete part costs. As expected, when a technology that adds resistors directly to the wiring layers is used, embedded resistors become economically viable when considerably fewer are integrated than for layer addition technologies.

For the applications considered, embedded bypass capacitors become economical when the capacitor density (number of discrete capacitors per square inch) reaches 7 – 8.5 capacitors/square inch or greater for reasonable panelization efficiencies when the dielectric replacement material with a cost of $0.10/square inch is assumed (these densities decrease if less expensive dielectrics can be used).

It must be reiterated that due to the opposing nature of many of the effects outlined in this chapter, the overall economic impact of replacing discrete passives with embedded passives, in general, yields application-specific results instead of general rules of thumb. We also need to point out several factors that should be kept in mind when interpreting the results in this chapter:

1) Several system implementation details are not addressed in this analysis including:
   i. Waste disposition in board fabrication – we only account for additional waste disposition costs associated with the fabrication of embedded passive boards in the profit margin differential.
   ii. Non-homogeneous panelization – some panel fabrication technologies and materials allow boards to be laid out on the panel with 90 degree relative rotations resulting in the potential for more boards on a panel, we have assumed homogeneous panelization in this analysis.
   iii. We have not considered the possibility that the conversion of discrete to embedded passives may allow some double-sided assemblies to become single sided thus saving significant assembly costs.

2) With any tradeoff analysis, the results are only as good as the input data, i.e., inaccuracies in the input data will change the results of the analysis. The software implementation of the methodology described in Sections 13.3.1 – 13.3.3 uses Monte Carlo analysis to model the impact of data input uncertainties.

13.6 References

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