

## **Optimizing Embedded Passive Content in Printed Circuit Boards**

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***Abstract*** – A genetic algorithms optimization approach is used in conjunction with a size/cost model to study the optimum mix of passives (resistors and capacitors) to embed within a printed circuit board on an application-specific basis. Using the models and solution approach developed in this paper, the effect of board size on the optimum embedded passive solution (minimum cost solution) is studied and an assessment of whether better system solutions can be found by varying or constraining the size of the board using several different criteria has been performed. Example optimization results for a GSM mobile phone are presented.

The analysis has shown that the system size limitation when embedded passives are used is not only dependent on the quantity, type, and electrical properties (capacitance and resistance) of the embeddable components, but is also very sensitive to layout specifications and the placement of the non-embeddable parts.

***Index Terms*** – *Embedded passives, integral passives, optimization, cost analysis, genetic algorithms.*

### I. INTRODUCTION

Embedded passives, also known as “integral” passives, are passive components buried within the layers of an interconnecting substrate (the substrate is the electrical interconnection between the components, e.g., a printed circuit board - PCB), [1]. Embedding passives frees board surface area to either shrink systems or add more active devices, and has the potential of increasing functionality and possibly performance in small electronic systems. Although capacitors, resistors and inductors are all candidates for embedding, most current interests are focusing on capacitors and resistors since they represent the majority of passive devices used on a circuit board. A generic single board computer is generally composed of 5% integrated circuits, 4% connectors, 40% capacitors, 33% resistors and 18% miscellaneous parts [2].

Embedded resistors and capacitors can be individually fabricated, and capacitors can also be manufactured in distributed planar form.

One significant concern of the embedded passive technology is whether the technology is economically feasible. The use of embedded passives is known to reduce assembly costs, shrink the required board size and negate the cost of purchasing and handling discrete passive components. However, these advantages must be traded off against the increased cost of boards fabricated with embedded passives and the decreased throughput and yield of the board fabrication process.

A model has been developed to perform the size/cost analysis on embedded passives in printed circuit boards. This model, described in [3] and summarized in Appendix A of this paper, captures the cost impact of a mixture of competing effects when embedded passives are present in the board including changes in board area, routing density requirements, board yield, and manufacturing costs. Due to the opposing nature of many of these effects, the overall cost impact of replacing discrete passives with embedded passives is not trivial to determine and, in general, yields application-specific results.

When passives are embedded into a PCB, one of the things the designer would like to know is what combination (type and quantity) of devices should be embedded to give the optimal cost (not every embeddable passive should necessarily be embedded). The model in [3] makes the assumption that as long as a device is embeddable then it should be embedded, not taking into consideration that there may be a specific combination of embeddable devices that could produce a better cost benefit while still meeting the design constraints.

Although several previous works have performed cost modeling for embedded passives, [3-8], optimizing embedded passive content based on cost minimization has only been addressed in [4]. The model developed by Power *et al.* [4], analyzed the embedding of resistors and capacitors in the form of an optimization problem targeted at choosing which discrete passives to embed based on an assumption of assembly and substrate manufacturing process details, and material properties. However the model in [4] did not considered embedding resistors and capacitors concurrently and optimized the resistors embedded based only on the availability of a finite selection of conductive inks. The model in [3], which we are using, also considers several important factors that were not included in [4], including, routing analysis, throughput variations, board and discrete passive yields, rework changes, and resistor trimming effects.

The analysis described in this paper has been used on an existing functional printed circuit board to determine the optimized embeddable resistors and capacitors that should be embedded to minimize cost. The optimization results were then examined by performing an analysis on system size/cost tradeoff to demonstrate the accuracy and validity of the results.

The next section of this paper describes the formulation and solution of the optimization problem. Section III provides an optimization study performed on the main board from a mobile phone. In Section IV the study goes beyond just finding the optimum embedded passive content for the mobile phone application and identifies the sensitivity of the solution to layout and placement constraints, and various assumptions about how the system cost results can change when passives are embedded.

## II. OPTIMIZATION APPROACH

In order to search for the optimum application-specific cost solution and embedded content, the model in [3] was implemented within a Genetic Algorithms optimization environment to determine the minimum application-specific system cost solution for embedding resistors and capacitors. This optimization method is used to demonstrate that the embedded passive content of a system can be optimized, and to explore the resulting optimized solution in order to draw general conclusions on the characteristics of optimized embedded passive content.

Genetic algorithms (GAs) are search algorithms based on the mechanics of natural selection and natural genetics [9]. GAs model the idea of the survival of the fittest and use interbreeding between surviving populations as the basis of its search strategy. Each new population represents possible solutions to a specified problem. The GA keeps creating new populations from the old by ranking each member of the old population and interbreeding the fittest individuals to create the new populations, which are closer to the optimum solution to the given problem. Occasionally random new data is added to the process to keep the population from stagnating. This random new data is characterized as mutation. Each new population that is created by this process is considered a generation. The particular GA implementation used to optimize the embedded passive process was developed by Chipperfield and Fleming [10] as a Genetic Algorithm Toolbox for use in MatLab.

The objective function for optimizing the embedded passive content is given by:

$$\text{Min } J = \underset{x \in L, y \in M, z \in N}{\text{Min}} (C_{\text{discrete}}(x, y, z) + P_{\text{board}}(x, y, z)) \quad (1)$$

where,

- J = System Cost
- L = [0, Total number of embeddable resistors]
- M = [0, Total number of embeddable non-bypass capacitors]
- N = [0, Total number of embeddable bypass capacitors].

$P_{\text{board}}$  (board price) and  $C_{\text{discrete}}$  (cost of all discrete passives) are defined in Appendix A. For nonnegative control, the objective function is obtained by using the following constraints (the symbols correspond to the model described in Appendix A):

- New wiring per layer pair:  $W_{\text{layer}_{\text{new}}}$  > 0
- Number of boards per panel:  $N_{\text{up}}$  > 0
- Area of new board:  $A_{\text{new}}$  in [3] > 0
- Discrete resistor value: > 0
- Discrete capacitor value: > 0
- Area of conventional board:  $A_{\text{conv}}$  > 0
- Number of I/O on conventional board:  $N_{\text{IO}_{\text{conv}}}$  in [3] > 0
- Number of discrete passives:  $N_{\text{discrete}}$   $\geq$  0

The parameters for the GA are defined in Table I.

TABLE I  
PARAMETERS FOR GA ANALYSIS [10]

Generation gap	0.8
Crossover rate	1
Mutation rate	1/NVAR <sup>1</sup>
Maximum number of generations	700
Insertion rate	0.9
Number of subpopulations	8
Migration rate	0.8
Number of generations/migration	20
Number of individuals/subpopulation	20

### III. EMBEDDED PASSIVE OPTIMIZATION FOR A MOBILE PHONE

The Genetic Algorithm optimization technique described in Section II was applied to an existing hand-held device, a SENDO M550 dual-band GSM folder-phone in order to determine the embedded passive content that minimizes the system cost. This section provides results and analysis of the system cost for the

<sup>1</sup> NVAR is the number of different resistor and capacitor categories. A category is determined by the value of the passive device and its physical attributes (e.g., bypass capacitors and singulated capacitors are two different categories).

SENDO M550 GSM cell phone main board.

### *A. Product Description*

The component of interest for this study is the main board of the SENDO M550 shown in Fig. 1. The breakdown of the relevant passive components and their associated characteristics and board design parameters are listed in Table II [11]. The distribution of specific resistors and capacitor values used for the analysis presented in this paper is assumed to be consistent with the component value distribution characterized by NEMI for portable devices found in [12].

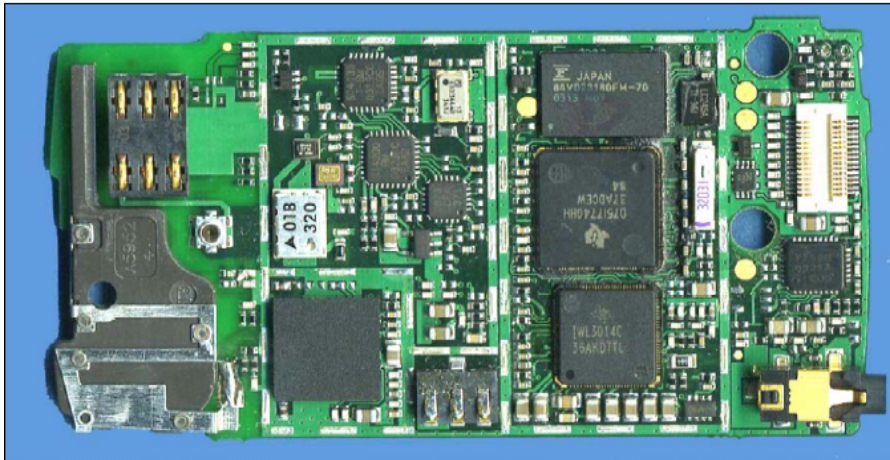


Fig. 1. Main board for SENDO M550 GSM cell phone showing the majority of the electronics in the product (photograph courtesy Portelligent).

TABLE II  
SENDO M550 GSM/GPRS PHONE MAIN BOARD CHARACTERISTICS AND DISCRETE RESISTOR AND CAPACITOR INVENTORY [11]

<b>Board Width (in)</b>	1.53			
<b>Board Length (in)</b>	2.98			
<b>Number of nets</b>	326			
<b>Number of holes</b>	1303			
<b>Assembly cost</b> (\$/discrete)	0.005			
<b>Part Type</b>	<b>Cost per part(\$)</b>	<b>Quantity</b>		
Resistors	0.001	55		
Capacitors ( $\leq 100$ nF)	0.005	134		
<b>Resistor Breakdown</b>	<b>Length (mils)</b>	<b>Width (mils)</b>	<b>Quantity</b>	
100 ohms	40	20	7	
500 ohms	40	20	24	
5000 ohms	40	20	7	
50000 ohms	40	20	14	
500000 ohms	80	50	2	
1000000 ohms	80	50	1	not embeddable
		<b>Total</b>	<b>55</b>	
<b>Total number of embeddable resistors</b>			<b>54</b>	
<b>Capacitor Breakdown</b>	<b>Length (mils)</b>	<b>Width (mils)</b>	<b>Quantity</b>	
bypass 100 pF	40	20	64	
bypass 1 nF	40	20	24	
bypass 15 nF	40	20	13	
bypass 30 nF	60	30	14	
bypass 100 nF	60	30	19	
non-bypass 250 nF	80	50	1	
non-bypass 1 microF	80	50	8	
non-bypass 2 microF	120	60	1	
non-bypass 9 microF	130	100	1	
non-bypass 10 microF	138	110	4	not embeddable
		<b>Total</b>	<b>149</b>	
<b>Total number of embeddable bypass capacitors</b>			<b>134</b>	
<b>Total number of embeddable non-bypass capacitors</b>			<b>11</b>	
<b>Total number of embeddable capacitors</b>			<b>145</b>	

### B. Optimization Results

This section discusses the results obtained from the optimization model for performing cost/size analysis of embedded passives on the SENDO mobile phone main board. The Portelligent information [11] provided an estimated board manufacturing cost, which was used to calibrate the model. This calibration was done by equating the board manufacturing cost in the model when no passive devices are embedded to that of Portelligent's board manufacturing cost estimate. This board manufacturing cost was used as a

TABLE III  
 SENDO M550 GSM/GPRS MAIN BOARD SYSTEM COST FOR VARIOUS COMBINATIONS OF EMBEDDED PASSIVE COMPONENTS PREDICTED BY THE NON-OPTIMIZED MODEL AND THE OPTIMIZED MODEL (BOARD SHRINKAGE ALLOWED). 18 X 24 INCH PANEL ASSUMED.

	Embedded Passives				System cost (\$)	
	Bypass Capacitors	Resistors $\leq 5 \text{ k}\Omega$	5 $\text{k}\Omega < \text{Resistors} \leq 50 \text{ k}\Omega$	50 $\text{k}\Omega < \text{Resistors} \leq 500 \text{ k}\Omega$		
Non-optimized model with no embeddable passives (Baseline Case)	0	0	0	0	34.43	No. of Layers = 6 No. of boards/panel = 65
Non-optimized model with all embeddable passives embedded	134	38	14	2	35.99	No. of Layers = 10 No. of boards/panel = 70
Optimized Model	134	38	6	0	32.37	No. of Layers = 6 No. of boards/panel = 70

benchmark throughout our modeling process. Table III shows the system cost for embedding the embeddable passive components in a SENDO M550 GSM phone main board when using the optimized cost model and the non-optimized cost model. The analysis of the SENDO main board assumes an additive embedded resistor technology<sup>2</sup> (e.g., MacDermid M-Pass technology [13]), and the use of a 10 nF/cm<sup>2</sup> (e.g., 3M C-Ply [14]) dielectric material for embedded capacitor fabrication. Appendix A provides the cost assumptions associated with the use of these technologies.

In the non-optimized cost model case, embedding all the embeddable passive components results in a higher system cost than not embedding any of the embeddable passives, \$35.99 as oppose to \$34.43 respectively. Both these system costs are significantly higher than the system cost obtained by choosing the best combination of resistors and capacitors to embed (\$32.37).

The optimum cost solution for the SENDO main board is realized when there are 134 bypass capacitors, 38 resistors  $\leq 5 \text{ k}\Omega$  and 6 resistors  $> 5 \text{ k}\Omega$  but  $\leq 50 \text{ k}\Omega$ .<sup>3</sup> Figures 2 through 4 show plots for the optimum cost solution for the SENDO main board. Figure 2 shows the effects of embedding resistors  $\leq 5$

<sup>2</sup> Additive embedded resistors do not require separate dedicate layer pairs (as with subtractive technologies). As the resistors are embedded (additively), they take up space on existing layers that could otherwise be used for routing - when enough resistors are added, enough space is blocked and either layer pair addition is necessary (to route everything) or the board has to get larger (to route everything).

<sup>3</sup> Note, embedding the non-bypass capacitors was never economically viable in the optimum solutions found for this example, even when the cost of the discrete capacitors replaced was as high as \$0.50 each.

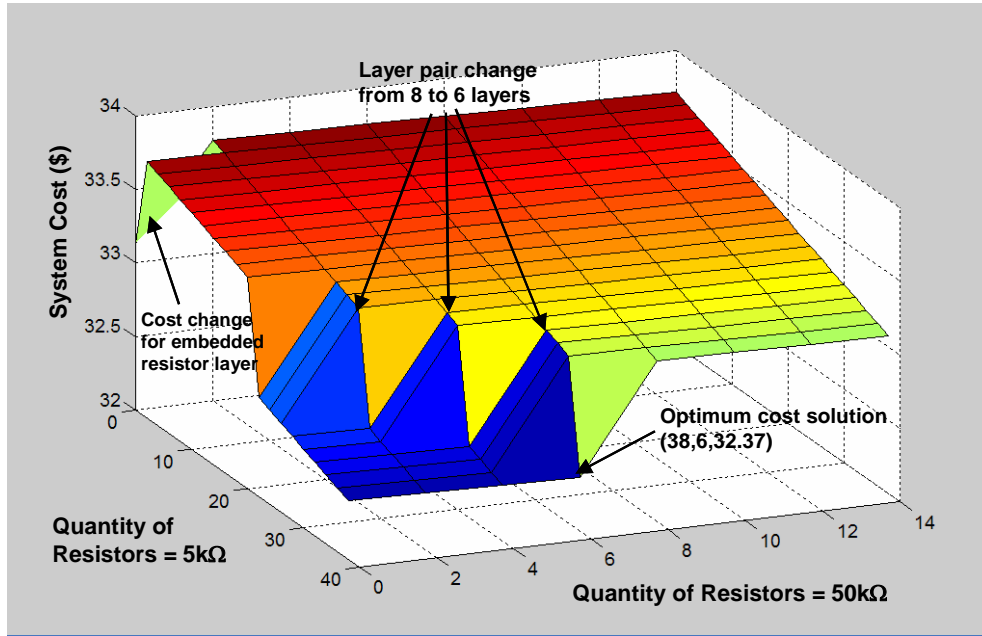


Fig. 2. System cost as a function of embedding resistors  $\leq 5$  k $\Omega$  and resistors  $\leq 50$  k $\Omega$ , quantities of other components are set at optimum values given in Table III.

k $\Omega$  and resistors  $\leq 50$  k $\Omega$  on the system cost for the SENDO cell phone main board. Note that the optimum solution occurs before the embedding of all resistors that are embeddable. Figure 3 shows the effects of embedding resistors  $\leq 5$  k $\Omega$  and bypass capacitors on the system cost for the SENDO cell phone main board. In this case it is shown that the optimum solution requires that all of the resistors  $\leq 5$  k $\Omega$  and bypass capacitors be embedded. Figure 4 shows the effects of embedding resistors  $\leq 50$  k $\Omega$  and bypass capacitors on the system cost for the SENDO cell phone main board. Figure 4 also shows that all bypass capacitors are embedded but only a portion of the resistors  $\leq 50$  k $\Omega$  should be embedded to obtain the optimum cost solution. Figures 2 through 4 show the importance of being able to obtain the optimal embedded content for a given application when embedding passives.



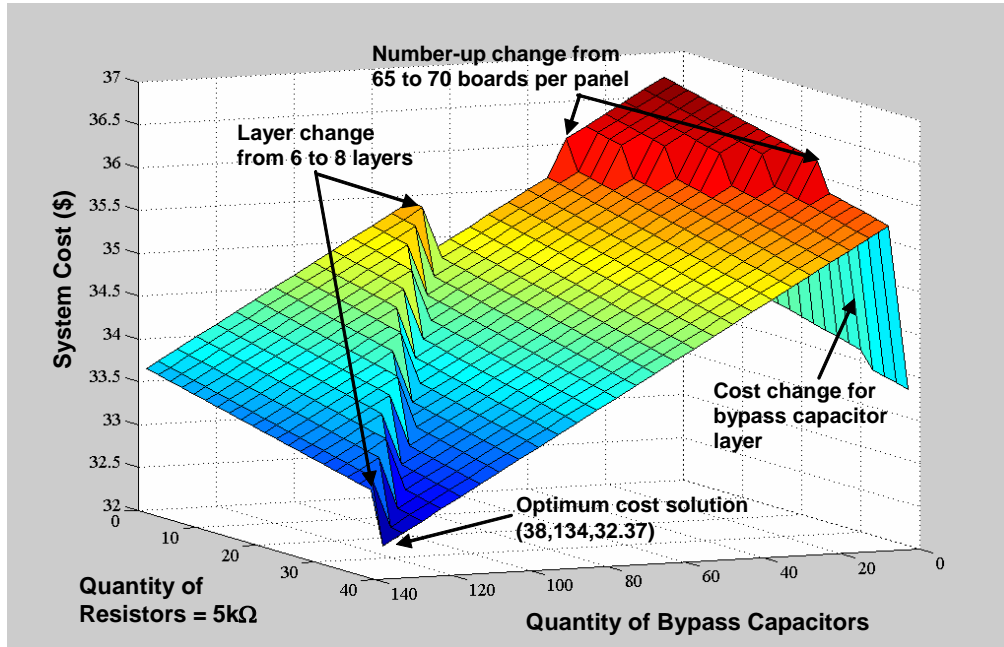


Fig. 3. System cost as a function of embedding resistors  $\leq 5 \text{ k}\Omega$  and bypass capacitors, quantities of other components are set at optimum values given in Table III.

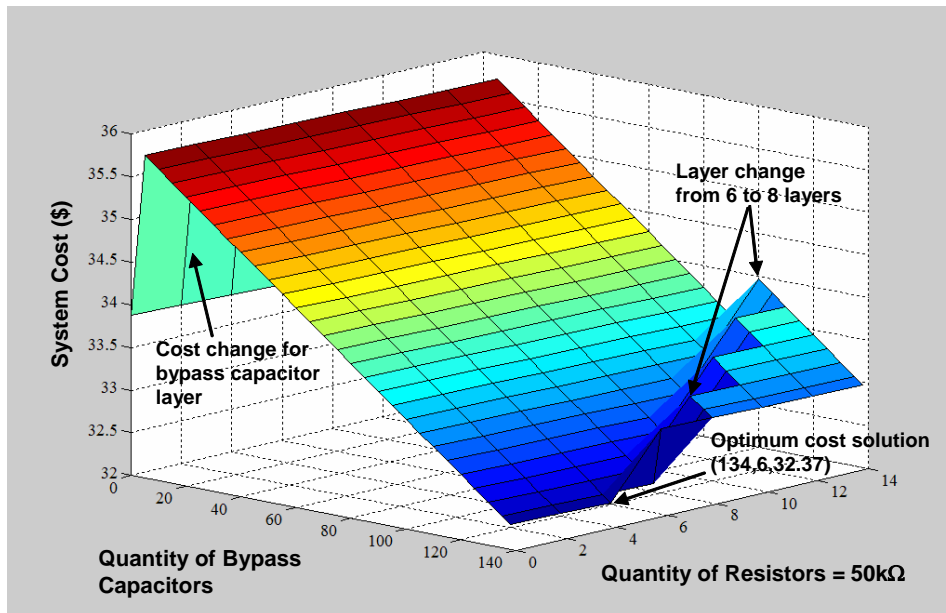


Fig. 4. System cost as a function of embedding resistors  $\leq 50 \text{ k}\Omega$  and bypass capacitors, quantities of other components are set at optimum values given in Table III.

#### IV. BOARD SIZE AND PLACEMENT IMPACTS ON THE OPTIMUM SOLUTION

There are several types of board area constraints that can be applied when optimizing embedded passive content in a board.<sup>4</sup> Specifically, two constraints need to be considered: maintaining a constant board area (board area remains unchanged as parts are embedded) or reducing the board area by the part footprint areas as parts are embedded (while preserving the board's original aspect ratio). The results presented in Section III represent the case where the board area decreases as parts are embedded. In this section we will more closely examine the effect of board size on the optimum solution (minimum cost solution) and assess whether better system solutions can be found by varying or constraining the size of the board in different ways. Besides holding the board area constant or allowing it to decrease as passives are embedded, two additional approaches were formulated to analyze the effects of board size on the system cost. The first approach was to select a range of fixed board sizes and determine the optimal embedded content for each size, then check to see if the selected fixed size/content combination is a physically possible solution. The second approach was to select a range of fixed board sizes and determine what content has to be embedded to allow the selected fixed board size to happen.

Determining the optimal embedded content for fixed board sizes was done by varying the size of the SENDO printed circuit boards by small increments. Each new board size was then subjected to the optimization model to determine the optimal embedded content. Note, the components that must be accommodated by the boards are a constant, i.e., they do not vary with the board size. Also, the passive components that are candidates for embedding is a constant that does not vary with board size. Note, no embeddable non-bypass capacitors were considered for embedding in the analysis in this section. An analysis was then performed to determine the conditions under which each result could be valid, i.e., to determine whether the selected board sizes and their optimized embedded content are physically possible to obtain.

Figure 5 shows the effects of board area on system cost for the SENDO GSM cell phone application. In Fig. 5 each data point was generated by selecting a fixed board area (the fixed areas range from 2 in<sup>2</sup> to the conventional board area of 4.56 in<sup>2</sup> when nothing is embedded) and running the optimization model not

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<sup>4</sup> In Section III we found the optimum embedded passive content for an application, however, it is the optimum under a set of constraints about how the board size is allowed to change when passives are embedded – and these constraints can be treated differently. In this section (and Appendix B) a more detailed board sizing analysis is performed to determine the conditions under which the optimum solution found in Section III is a reasonable solution.

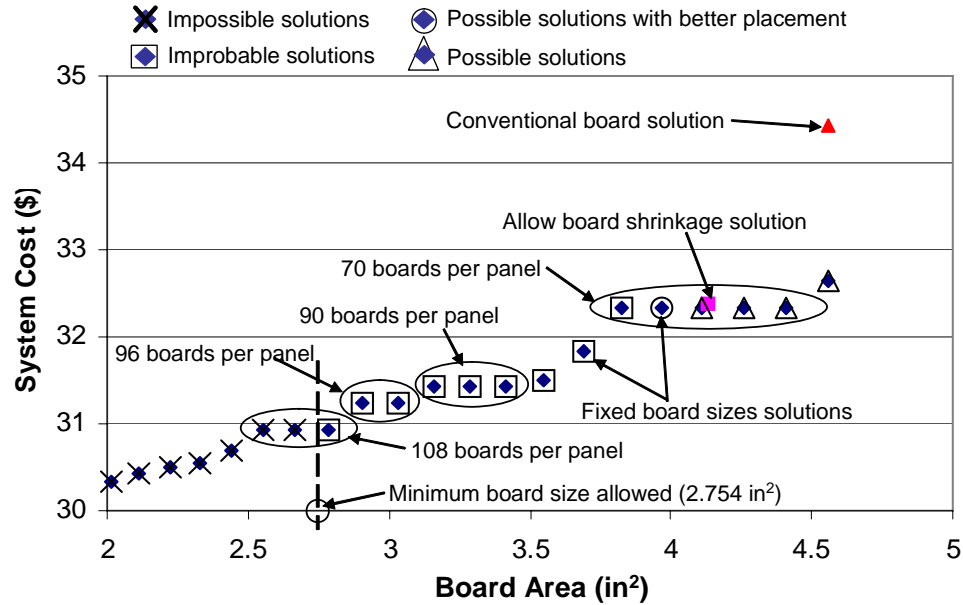


Fig. 5. Effects of fixed board sizes on system cost for SENDO GSM cell phone application, where the optimized embedded content was determined for each fixed board size. Possible and impossible board areas for the SENDO GSM application main board are also indicated. 18 x 24 inch panel assumed.

allowing board shrinkage (not allowing the model to shrink the board as passives are embedded) to determine the content and system cost. The “Allow board shrinkage solution” in Fig. 5 represents the optimized solution that shrinks the conventional board as embeddable passives are embedded (\$32.37 from Table III). Assuming a single material (one value of resistivity) is available to make embedded resistors, the decrease in system cost for the fixed board size solutions is primarily governed by the changes in the number of boards that can be fabricated per panel area (number-up). In cases where the number of boards produced per panel is constant, the system cost remained constant (even when the board size was decreased).

The optimal embedded content remains the same in all cases (134 bypass capacitors, 38 resistor of resistive value less than 5 kΩ and 14 resistors of resistive value between 5 kΩ and 50 kΩ) except board area 2.12 in<sup>2</sup> where the number of resistors with resistive values between 5 kΩ and 50 kΩ is 13 and for board area 2.01 in<sup>2</sup> where the number of resistors with resistive values between 5 kΩ and 50 kΩ is 12.

Many solutions shown in Fig. 5 appear to be better (smaller and less expensive) than the optimal solution identified in Section III (the “Allowed board shrinkage solution” in Fig. 5). This is because these additional solutions depend on relaxing various constraints that the optimization was bound by. The key constraint that is relaxed in order to enable the additional solutions is the placement of parts. Figure 5

indicates that the “Allow board shrinkage solution” represents the minimum system cost within the set of solutions that are possible with the same or better placement of the non-embeddable parts.<sup>5</sup> As small parts are embedded the relative efficiency of the overall placement decreases or the packaging density decreases (see Appendix B), “better placement” in Fig. 5 means preserving the packaging density of the conventional solution when parts are embedded. Improbable solutions have a higher packaging density than the conventional solution, i.e., they assume a more efficient tiling of the non-embedded parts in the layout. Smaller placement ratios (ratios that are improbable) can only be attained if the layout specification for the conventional system is ignored and the placement of non-embeddable parts are optimized to render a greater packaging density than that of the conventional system – performance and functionality constraints may not allow this.

Finally the absolute minimum physical size constraint for the SENDO application with every embeddable part embedded is  $2.754 \text{ in}^2$ , which is the total assembly spacing and assembly area required to accommodate all the non-embedded embeddable devices on the surface of the SENDO application (assuming everything tiles together perfectly). The embedded passive content at  $2.754 \text{ in}^2$  is 134 bypass capacitors, 38 resistors of resistive value less than  $5 \text{ k}\Omega$  and 14 resistors of resistive value between  $5 \text{ k}\Omega$  and  $50 \text{ k}\Omega$ . This means that the solutions in Fig. 5 below  $2.754 \text{ in}^2$  are never physically possible under any conditions.

The detailed construction of the constrained cases shown in Fig. 5 is provided in Appendix B.

## V. SUMMARY AND DISCUSSION

This paper demonstrates application-specific optimization of embedded passive content and its potential system cost benefits.

The analysis shows that the “Allow board shrinkage solution” represents the minimum system cost within the set of solutions that are possible with the same or better placement of the non-embeddable parts. If systems have placement ratios (the ratio of the board area to the sum of the footprints of all the parts that

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<sup>5</sup> The system cost for the case where boards shrink as parts are embedded is slightly greater than the system cost for the fixed board sizes with the same number of boards produced per panel (70 boards per panel range). This is due to the fact that the embedded passive content for the allow board shrinkage solution has only 6 resistors of resistive value between  $5 \text{ k}\Omega$  and  $50 \text{ k}\Omega$  embedded as oppose to 14 resistors in the fixed board size solution. The assembly, rework, procurement and AOI cost associated with the 8 resistors that are not embedded in the “Allow board shrinkage solution” increases the system cost by half a cent (\$0.005).

are not embedded) that fall within the set of solutions that are improbable even with better placement then, it is possible to obtain system costs that are less than that of the “Allow board shrinkage solution”, however given that the passives that are embedded are usually much smaller than the non-embeddable parts, better placement solutions (smaller placement ratio) are considered improbable. Smaller placement ratios (ratios that are improbable) can only be attained if the layout specification for the conventional system is ignored and the placement of non-embeddable parts are optimized to render a greater packaging density than that of the conventional system – performance and functionality constraints may not allow this.

The analysis has also shown that the system size limitation when embedded passives are used is not only dependent on the quantity, type, and electrical properties (capacitance and resistance) of the embeddable components but is, in fact, more dependent on layout specifications and the placement of the non-embeddable parts. From the analysis performed it is evident that the optimum system cost solution does not generally result in the minimum possible size for the system. This analysis shows that it is possible to attain smaller board areas for a printed circuit board application if the possibility of better placement of surface mount devices is considered. It also shows that when the layer count increases, the packaging density increases thus providing a better (smaller) placement ratio for the system since more passives can be embedded on a smaller board area, however this better placement ratio comes at a higher system cost due to layer pair addition. This analysis shows that even though the optimization model does in fact provide the minimum system cost (under the placement constraints summarized in the preceding paragraph) it does not provide the minimum size. This is due to the fact that the optimization of the layout of parts on the surface of the system is not considered within the methodology described in this research.

The analysis in this paper constrained the design options available for embedding capacitors and resistors by only considering a limited number of materials. There are a range of dielectric materials available for embedding bypass capacitors that vary in properties and price. In the case of embedded resistors, we have assumed an additive approach, which is generally much less expensive than subtractive approaches. For resistors, multiple materials (with differing resistivities) may be available for embedding resistors into a single board. The board area necessary to embed a resistor depends on the resistivity of the material used to make the embedded resistor. Optimization of embedded content with multiple material options would be an obvious extension of this work.

APPENDIX A – COST MODEL FORMULATION

The model formulation described in this appendix is a summary of a previously published model, [3]; therefore, this appendix only provides the primary equations and associated variable descriptions. For a derivation of this model and a detailed discussion of the assumptions used, see [3].

The effective cost of a discrete passive component is given by,

$$C_{\text{discrete}} = \sum_{i=1}^{N_{\text{discrete}}} \left[ P_{\text{discrete}_i} + C_{\text{handling}_i} + C_{\text{assembly}_i} + C_{\text{AOI}_i} + (1 - Y_{\text{assembly}_i}) (C_{\text{assbly rework}_i} + P_{\text{discrete}_i} + C_{\text{handling}_i}) + (1 - Y_{\text{functional}_i}) (C_{\text{func rework}_i} + P_{\text{discrete}_i} + C_{\text{handling}_i}) \right] \quad (\text{A.1})$$

where

$P_{\text{discrete}}$  = purchase price of a discrete passive component

$C_{\text{handling}}$  = storage and handling costs associated with a discrete passive component

$C_{\text{assembly}}$  = the cost of assembly of a discrete passive component (per site)

$C_{\text{AOI}}$  = cost of inspecting a discrete passive component (per site)

$Y_{\text{assembly}}$  = assembly yield for discrete passive components

$Y_{\text{functional}}$  = functional yield of discrete passive components

$C_{\text{assbly rework}}$  = cost of reworking an assembly fault (per site)

$C_{\text{func rework}}$  = cost of diagnosing and reworking a functional fault (per site)

$N_{\text{discrete}}$  = the number of discrete passives that are converted to embedded passives.

The price per board is given by,

$$P_{\text{board}} = \frac{(1 + M)}{N_{\text{up}}} \left[ C_{\text{layer pair}} A N_{\text{layers}} + N_{\text{bypass cap layers}} C_{\text{bypass cap layer}} + N_{\text{embedded cap layers}} C_{\text{embedded cap layer}} \right] \quad (\text{A.2})$$

where

$M$  = board profit margin

$C_{\text{layer pair}}$  = cost per unit area per layer pair given by (A.3)

$A$  = the board area

$N_{\text{up}}$  = number up, number of boards that can be fabricated on a panel

$N_{\text{layers}}$  = total number of layers (wiring and reference) in the board.

$N_{\text{embedded cap layers}}$  = number of embedded capacitor layers (for non-bypass capacitors)

$N_{\text{bypass cap layers}}$  = number of bypass capacitor layers

$C_{\text{embedded cap layers}}$  = cost of embedded capacitor layers (for non-bypass capacitors), which is given by the sum of the processing and material costs =  $C_{\text{ecl process}} + C_{\text{ecl material}}$

$C_{\text{bypass cap layers}}$  = cost of bypass capacitor layers, which is given by the sum of the processing and material costs =  $C_{\text{bcl process}} + C_{\text{bcl material}}$ .

The embedded board layer pair cost in (A.2) is given by,

$$C_{\text{layer pair}} = C_{\text{layer pair}_{\text{conv}}} + (C_{\text{resistor material}}) \left( N_{\text{up}} \right) \sum_{i=1}^{N_{R'}} \text{Area}_{R_i} + N_{R'} C_{\text{trim}} N_{\text{up}} + C_{\text{print}} \quad (\text{A.3})$$

where the sum in (A.3) is taken over all embedded resistors in the particular layer pair of interest ( $N_{R'}$ ), and

$C_{\text{layer pair}_{\text{conv}}}$  = cost per unit area of per layer pair for the conventional (no passives embedded) board

$C_{\text{resistor material}}$  = cost per unit area of the resistive material printed on the wiring layers to create embedded resistors

$C_{\text{trim}}$  = the average cost of trimming one printed resistor<sup>6</sup>

$C_{\text{print}}$  = the average cost of printing or plating all embedded resistors onto one layer pair

$N_{R'}$  = number of embedded resistors on a particular layer of interest

$\text{Area}_{R_i}$  = area occupied by the  $i^{\text{th}}$  embedded resistor, see [3] for calculation.

As discrete passive components are converted to embedded passives, the physical size of the board can either remain fixed or be allowed to decrease by the layout area associated with the discrete passives given by,

$$A = A_{\text{conv}} - \sum_{i=1}^{N_{\text{discrete}}} (l_i + S)(w_i + S) \quad (\text{A.4})$$

where

$S$  = the minimum assembly spacing

$l_i$  and  $w_i$  = the length and width of the  $i^{\text{th}}$  discrete passive

<sup>6</sup> In the analysis performed in this paper, 85% of the resistors were assumed to require trimming (the model allows this percentage to be varied). The cost of trimming was assumed to be \$0.002/trimmed resistor.

$A_{conv}$  = the conventional board area.

The number of wiring layers,  $N_{layers}$ , appearing in (A.2) also has to be calculated. The calculation of the number of wiring layers is too complex for this brief appendix, but is covered in detail in [3]. The calculation of  $N_{layers}$  depends on the wiring resources available on each layer pair  $W_{layer_{new}}$ , as well as wiring efficiency, number of I/O, and other application-dependent parameters. The values of the various parameters used in the cost modeling are given in Table A.I.

TABLE A.I  
DEFAULT VALUES USED IN COST CALCULATIONS (18 X 24 INCH PANEL ASSUMED)

Embedded Capacitor Material Cost (\$/ft <sup>2</sup> ) – non-bypass capacitors	$C_{ecl\ material}/(\text{panel area})$	\$14.98 (\$0.104/in <sup>2</sup> )
Embedded Capacitor Processing Cost (\$/panel) – non-bypass capacitors	$C_{ecl\ process}$	25
Bypass Capacitor Processing Cost (\$/panel)	$C_{bcl\ process}$	35
Resistor Printing Cost/Layer (\$/layer pair)	$C_{print}$	7.43
Cost of Bypass Capacitor Material (\$/ft <sup>2</sup> )	$C_{bcl\ material}/(\text{panel area})$	14.4 (\$0.10/in <sup>2</sup> )
Conventional Panel Cost (\$/ft <sup>2</sup> /layer pair)	$C_{layer\ pair_{conv}}$	12.5
Embedded Resistor Material Cost (\$/in <sup>2</sup> )	$C_{resistor\ material}$	0.08
Trimming Cost/Resistor (\$/embedded resistor)	$C_{trim}$	0.002
Passive Conversion Cost (\$/passive)	$C_{handling}$	0.015
Assembly Cost (\$/discrete)	$C_{assembly}$	0.075
AOI (\$/discrete)	$C_{AOI}$	0.0004
Assembly Rework Cost (\$/site)	$C_{assbly\ rework}$	4
Functional Rework Cost (\$/site)	$C_{func\ rework}$	4
Assembly Yield/discrete	$Y_{assembly}$	99.99%
Passive Yield/passive	$Y_{functional}$	99.999%
Conventional Board Profit Margin	Used to compute M, see [3]	15.7%



#### APPENDIX B – DETAILED ANALYSIS OF BOARD LAYOUT AND PLACEMENT

This appendix provides a detailed analysis of the board layout and placement constraints that enable the grading of the solutions shown in Fig. 5.

The modeling approach described in Appendix A and [3] is a “relative” model. It is relative in the sense that it does not know exactly how much wiring is required to route the conventional version of the board, only the resulting size and number of layers. The analysis then estimates the properties of the board with embedded passives in it relative to the conventional board (the model calculates changes only). The placement of the parts on the conventional board is not an input to the model, i.e., the model is designed to function without it. Therefore, a detailed analysis of the viability of the modified board areas requires the detailed development that is described in this appendix.

In order to assess the likelihood that various solutions are realizable, the following ratios are used to determine the maximum likely and minimum allowable board sizes. The conventional board ratio (CR), is the ratio of the conventional board area to the sum of the assembly footprints of all the parts. Where a part’s assembly footprint is its physical area plus the space around it required for its assembly (assembly spacing). CR is the inverse of the “packaging density” of the conventional board.

$$CR = \frac{CB_A}{AA_C}, \text{ the conventional board ratio} \quad (B.1)$$

where  $CB_A$  is the conventional board area and  $AA_C$  is the sum of the assembly footprints for all parts for the conventional board (nothing embedded). The allow board shrinkage ratio (SR), is the ratio of the “Allow board shrinkage solution” area to the sum of the footprints of all the parts that are not embedded. SR is the inverse of the “packaging density” for the “Allow board shrinkage solution”.

$$SR = \frac{SB_A}{AA_{SB}}, \text{ allowed board shrinkage ratio} \quad (B.2)$$

where  $SB_A$  is the “Allow board shrinkage solution” board area and  $AA_{SB}$  is the sum of the assembly footprints for all non-embedded parts for the “Allow board shrinkage solution”.

The minimum allowable board area ( $MIN_{BA}$ ) and the maximum likely board area ( $MAX_{BA}$ ) are determined from,

$$\begin{aligned} \text{MIN}_{BA} &= \text{MIN}[(\text{CR})AA_{SB}, (\text{SR})AA_{SB}] \\ \text{MAX}_{BA} &= \text{MAX}[(\text{CR})AA_{SB}, (\text{SR})AA_{SB}] \end{aligned} \tag{B.3}$$

Initially we will analyze in detail the solutions for the fixed board sizes that produce 70 boards per panel and compared them to the “Allow board shrinkage solution”. This analysis involves the following steps:

1. Calculate the conventional board ratio (CR). This ratio was used to determine the minimum board size that is allowable for a given fix board area solution that preserves the conventional board surface mount passive component placement.
2. Calculate the allow board shrinkage ratio (SR). This ratio was used to determine the maximum board size that is allowed for a given fix board area solution that preserves the allow board shrinkage surface mount passive component placement.
3. The embedded content needed to obtain the minimum and maximum board size allowed was determined and the system cost for that particular embedded content was plotted. CR and SR determine the minimum allowable and maximum likely board sizes respectively. Note, not all the fixed board areas in Fig. 5 will fall within the minimum allowable and maximum likely board size (this will be expanded upon later in this Appendix).

For the SENDO application, the ratio of conventional board area to total surface assembly area of conventional board (CR) is 1.40 and the ratio of allow board shrinkage solution board area and total surface assembly area of allow board shrinkage solution (SR) is 1.49. If perfect placement of all non-embedded parts was possible, the ratio of the board area and the total assembly area would be 1. The ratio for the embedded case is greater than that of the conventional case due to the absence of small embedded passives. This increase in ratio for the embedded case can be better understood using the schematic presented in Fig. B.1. By embedding the smaller embeddable devices the packaging density for the system decreases because the placement can't change very much when just small parts are removed, which results in an increase in the allow board shrinkage ratio (SR). If it is assumed that the relative placement of the surface mount devices on the conventional board is constrained by a performance specification and should be kept constant, then the ratios, CR and SR, would be kept constant to maintain the same relative placement for

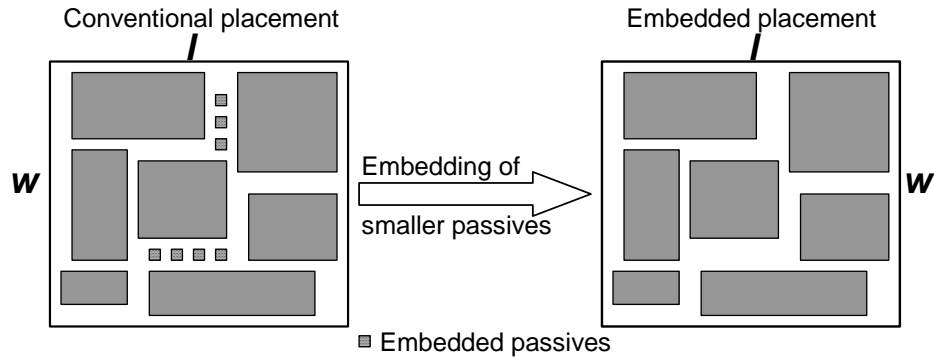


Fig. B.1. Effects of embedding smaller devices on packaging density (embedding the embedded passives on the left may cause no change in the board size because of placement constraints driven by the larger parts).

the printed circuit board application (i.e., the relative locations of parts may be important to the performance and/or functionality of the system). These ratios were used to determine the minimum allowable and maximum likely allowable board area for a particular fix board size. These maximum and minimum board areas were found by multiplying each ratio, CR and SR, by the total surface assembly area required for the “Allow board shrinkage solution”.

The system cost at the minimum and maximum board size was determined by varying the embedded passive content for the system and allowing the fixed board size to vary. Fig. B.2 is the analysis corresponding to one of the points from Fig. 5 that is in the 70 boards per panel solution. The analysis performed on the fixed boards sizes that are illustrated in Fig B.2 through Fig. B.5 illustrates the effects of varying constraints (in this case board size) on the optimal solution for a given system. Fig. B.2 shows an analysis of the fixed board size of  $4.26 \text{ in}^2$  on the system cost for the SENDO application and the possible ranges of board sizes that are attainable. In Fig. B.2 it is observed that the fixed board area of  $4.26 \text{ in}^2$  and the allow board shrinkage solution area of  $4.13 \text{ in}^2$  are both greater than the maximum board area of  $4.103 \text{ in}^2$ . This is due to the fact that the placement of passive devices (utilization of surface area) is not optimized for this particular case. It is also observed that the system cost at both the minimum (\$33.31) and maximum (\$34.25) board areas are greater than that of the “Allow board shrinkage solution” and the fixed board area solution (\$32.37).

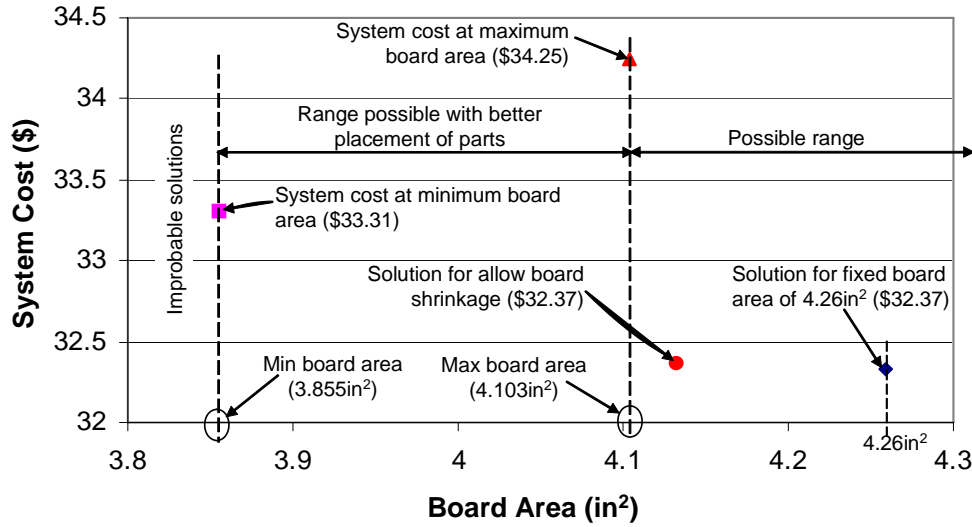


Fig. B.2. Effects of board size 4.26 inch<sup>2</sup> on system cost for SENDO application (70 boards / panel) ( $AA_{SB} = 2.76 \text{ in}^2$ ). 18 x 24 inch panel assumed.

This increase in the system cost is a direct result of moving away from the optimal embedded content to obtain these board areas. The range between the minimum and maximum board areas is considered possible with “better” placement (i.e., better placement than the “Allow board shrinkage solution”) of all components, and the board areas below the minimum board area are considered improbable since they would require better placement than the conventional system.

Similar to Fig. B.2, Fig. B.3 through Fig. B.5 show the effect that the fixed board areas that produce 70 boards per panel have on the system cost and which of these areas are physically possible. In Fig. B.3 it is observed that the fixed board area of 4.11 in<sup>2</sup> has the same general characteristics as the fix board area of 4.26 in<sup>2</sup> shown in Fig. B.2.

The differences are that the fixed board area of 4.11 in<sup>2</sup> is much closer to the maximum board area and the system cost at the minimum and maximum board area are slightly greater in Fig. B.3. In Fig. B.4 the fixed board area of 3.97 in<sup>2</sup> falls between the minimum and maximum board area. This means that better placement of all parts is required if this board area is going to be valid. Also when the board size is increased by the area amount of all the embeddable non bypass capacitors and resistors that were not embedded in the solution, the total area required is 4.076 in<sup>2</sup>, which is less than the maximum board area of 4.103 in<sup>2</sup>, therefore there is no system cost at the maximum board area in Fig. B.4. The system cost at the minimum board area is observed to be higher than that found in Figs. B.2 and B.3. In Fig. B.5 it is shown

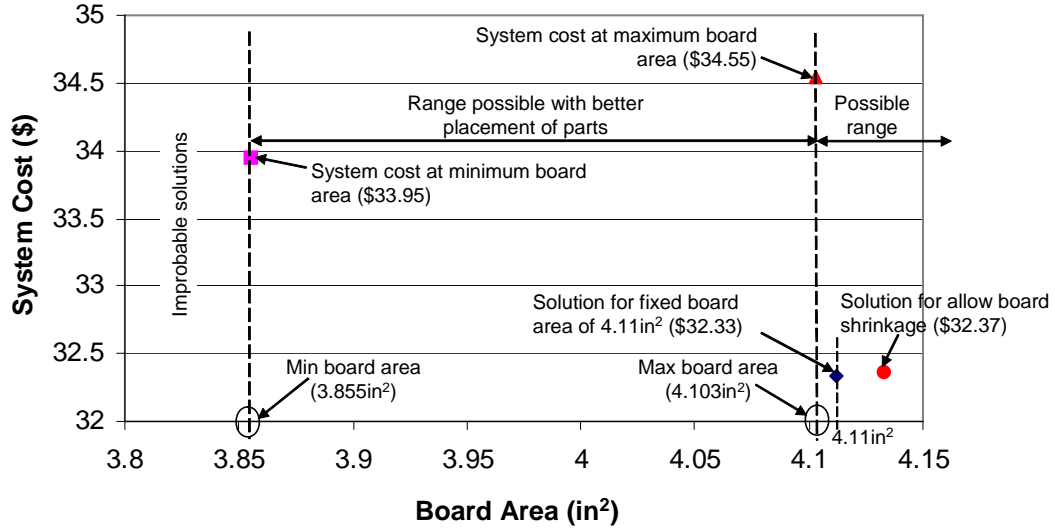


Fig. B.3. Effects of board size 4.11 inch<sup>2</sup> on system cost for SENDO application (70 boards/ panel) (AA<sub>SB</sub> = 2.76 in<sup>2</sup>). 18 x 24 inch panel assumed.

that the fixed board area of 3.83 in<sup>2</sup> falls into the improbable range of board areas. It also shows that when the board area of 3.83 in<sup>2</sup> was allowed to vary by varying the embedded content the minimum board area was not attainable.

The ratio analysis was conducted for all the SENDO fixed board areas presented in Fig. 5. This ratio analysis is depicted in Fig. B.6 where the conventional board ratio (CR) and the allow board shrinkage ratio

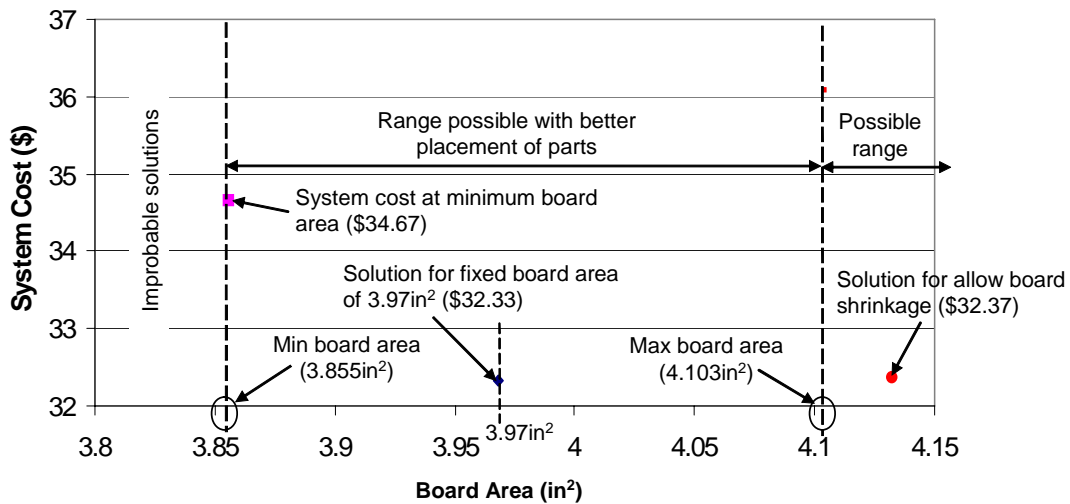


Fig. B.4. Effects of board size 3.97 inch<sup>2</sup> on system cost for SENDO application (70 boards/ panel) (AA<sub>SB</sub> = 2.76 in<sup>2</sup>). 18 x 24 inch panel assumed.

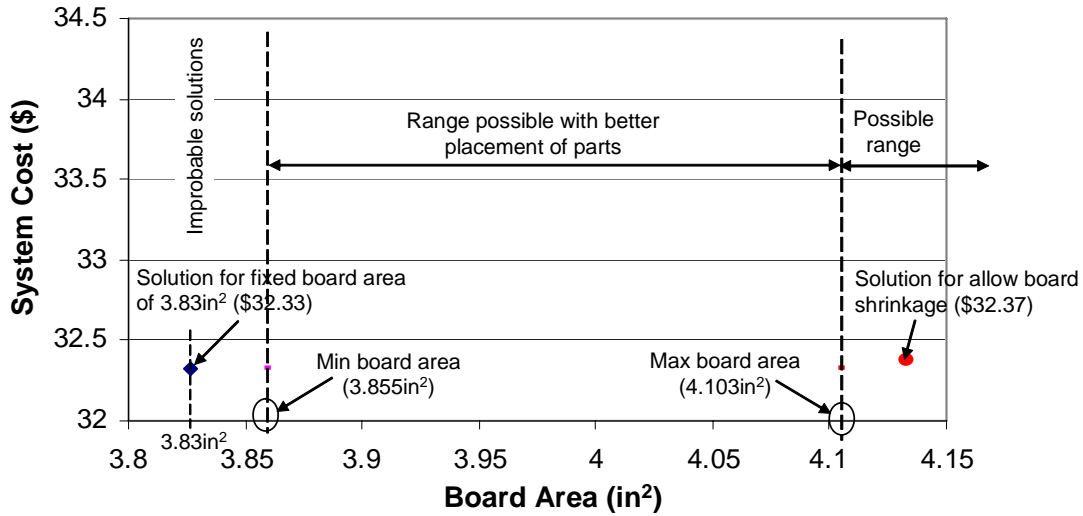


Fig. B.5. Effects of board size 3.83 inch<sup>2</sup> on system cost for SENDO application (70 boards/ panel) ( $AA_{SB} = 2.76 \text{ in}^2$ ). 18 x 24 inch panel assumed.

(SR) are shown. This analysis shows that only a few of the board areas from Fig. 5 actually fall within the possible range of board area that can be manufactured.

Figure B.1 shows a case where the placement ratio<sup>7</sup> for the conventional placement is smaller than that of the embedded placement since more of the assembly area is utilized in the conventional case and the

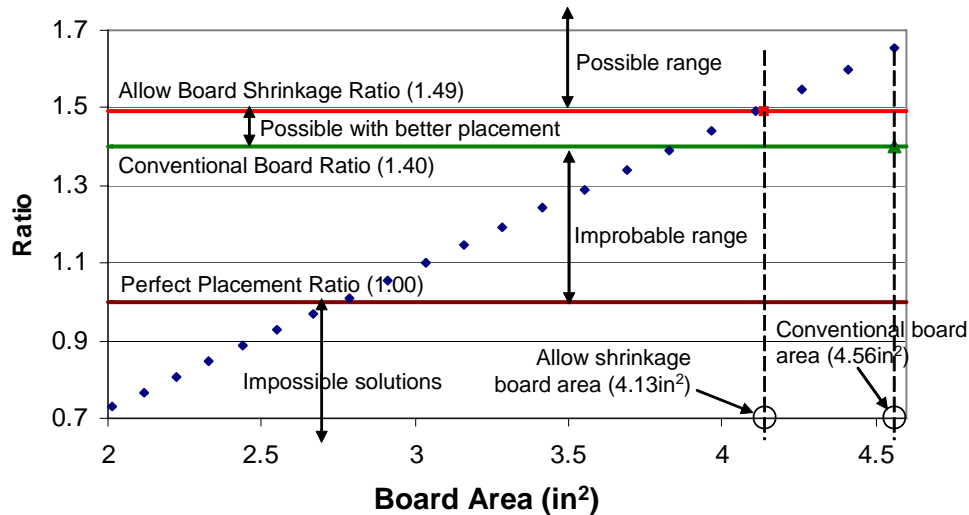


Fig. B.6. Ratio analysis for fix board areas for the SENDO GSM cell phone application. The points on the diagonal line of points represents the sum of the assembly footprints for all the non-embedded parts in the SENDO application, i.e., the slope of the diagonal line of points is  $AA_{SB}$  (see (B.2) and associated discussion). 18 x 24 inch panel assumed.

board area remains the same. Figure B.7 provides an example of how a placement ratio that is less than that of the conventional system can be obtained. In this case it is possible that the ratio for embedded placement is smaller than that of the conventional placement since the board area in the embedded case is reduced by embedding the smaller passives devices. For the most part, the embeddable passive devices are much smaller than the non-embeddable devices and the possibility of getting a smaller placement ratio is dependent on the placement of embeddable passive devices remaining on the surface of the original board. Figure B.7 demonstrates one of the cases in which it may be possible to obtain a smaller placement ratio than that of the conventional system.

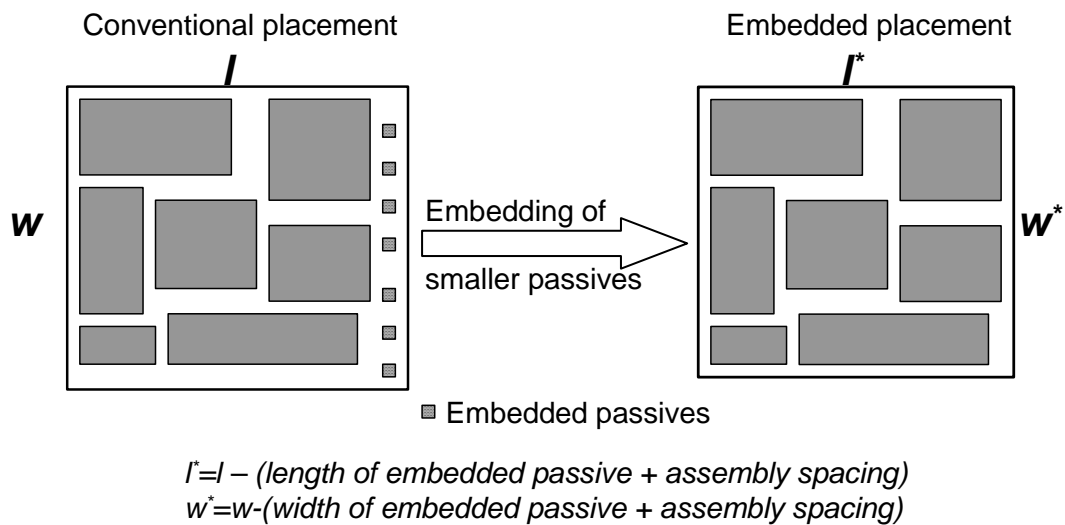


Fig. B.7. Possibility of getting a new placement ratio that is less than that of the convention board ratio (CR).

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